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Wide Dynamic Range, Highly Accurate, Low Power CMOS Potentiostat for Electrochemical Sensing Applications

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Wide Dynamic Range, Highly Accurate, Low Power CMOS Potentiostat for Electrochemical Sensing Applications

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DEDICATION

I would dedicate this thesis to my loving grandparents Susheela and Krishna Shetty, and my parents Sukanya Kumari and Mohan Kumar and my uncle Ravindranath, who have supported me in each and every step of my life.

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ABSTRACT

Diabetes is a global epidemic that threatens the health and well-being of hundreds of millions of people. The first step in patient treatment is to maintain healthy glucose levels, requiring continuous and accurate monitoring. Modern glucose monitoring systems use electrochemical methods that are invasive, painful and time-consuming and often results in dangerous fluctuations in glucose levels going undetected. Recent developments in biomedical sensors and CMOS integrated circuit technologies have led to the realization of non-invasive and minimally invasive glucose monitoring systems that overcome these limitations and may be implantable.

An implantable glucose sensor scheme can also be modified to detect and quantify other physiological factors such as lactate, oxygen, and pH. A potentiostat is an integral part of a glucose sensor that controls the potential difference between the two electrodes and acquires sensor signals for the signal processing unit that collects and processes the data to transmit to a wireless device. A number of potentiostat circuits have been introduced for glucose monitoring devices but many suffer poor accuracy and improved measurement sensitivity is needed.

This work focuses on addressing the issues in existing potentiostat configurations and develops a low power, compact potentiostat with wide dynamic range and high accuracy that can not only be used for glucose monitoring systems but also for other physiological factors and electrochemical sensing applications with considerable improvements in sensitivity and dynamic range to meet future needs.

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CHAPTER 1–INTRODUCTION

Diabetes, a disease that is caused due to high or low blood glucose level, is affecting millions of people today. According to American Diabetes Association, Diabetes remains the seventh leading cause of death in the United States responsible for more than hundred thousand deaths each year. There are 5 different types of diabetes but a majority of people are affected by type1, type2 diabetes. Type1 is caused due to insufficient production of insulin and is mainly found in children but can be developed in adulthood as well. Type 2 is produced due to improper utilization of the insulin released, by the body. This is mainly found in adults and about 90% of people with diabetes are type 2.

Most of the people with diabetes do not have any symptoms except for hyperglycemia and hypoglycemia. Hyperglycemia is a condition caused due to high blood glucose level. It can lead to significant organs damage and further complications. Hypoglycemia is a condition caused due to the low blood glucose level. Frequent glucose monitoring is an essential part of avoiding the complications of diabetes. Different parts of the body affected by diabetes results in cardiovascular diseases and heart attack, eye problems leading to blindness, kidney problems, sexual issues and problems related to circulation and scarring

1.1 Importance of Blood Glucose Monitoring

Managing blood glucose concentration is one of the challenges of monitoring diabetes. The blood glucose level must be daily controlled to avoid complications. Increased blood glucose level can be minimized by taking a dietary supplement or oral medication and lower blood glucose level can be compensated by injecting insulin or other appropriate measures can be taken to bring the blood glucose level to normal. The sugar level in the blood varies continuously throughout the day and from person to person due to a number of factors like age, health condition illness and personal habits. It seems to be lower before the meal and higher soon after the meal and settles down low eventually. Diet, exercises, fasting, stress and other factors continuously affect the blood glucose level of the body. Continuous glucose monitoring of glucose is particularly useful for type 1 diabetic patients. It helps take optimal treatment decision

for patients and also provides information about direction, magnitude, duration, frequency and causes of fluctuation of blood glucose levels thus providing greater insight into patient's blood glucose level. So it is important to continuously monitor the blood glucose level throughout the day.

1.2 Different Types of Blood Glucose Monitoring

There are three different methods of blood glucose monitoring:

i. Invasive Method
ii. Minimally Invasive Method
iii. Non-Invasive Method

1.2.1 Invasive Method

This method involves measuring the glucose level with the help of a glucose meter which requires a blood sample. Blood samples are taken by pricking the finger or thin lancelet placed subcutaneously, involves pain or discomfort and risk of infection resulting in poor patient compliance. The issue of regularly checking the blood glucose level for many diabetic patients makes this an inefficient method. Figure 1 depicts glucose measurement by taking blood sample.

Figure 1: Glucose measurement by taking a blood sample [27].

1.2.2 Minimally Invasive Method

Minimally invasive techniques involve subcutaneous sensors to measure the glucose concentration of bodily fluid such as tears, sweat, interstitial fluid, through an enzymatic reaction. An implanted glucose sensor can continuously monitor glucose level time by time and warn the patients when it exceeds the limits. Eventually, this sensor can be coupled with an implantable insulin pump for automatic injection of insulin when required. However, this involves discomfort and continuous calibration requirements and the risks of biofouling. Figure 2 represents a minimally invasive glucose monitoring system.

1.2.3 Non-Invasive Method

The Non-invasive method involves the determination of glucose concentration without using blood or any other bodily fluids. It is based on the ability of glucose molecules to interact with physical and chemical processes happening in the body. Non-invasive methods fall into two categories, optical and transdermal. The optical method involves the interaction of light and transdermal method involves the interaction of physical energy. According to FDA-Food and Drug Administration, the non-invasive devices are only 15% accurate. But new techniques are being developed with improved accuracy. Figure 3 shows the method of glucose sensing using contact lens.

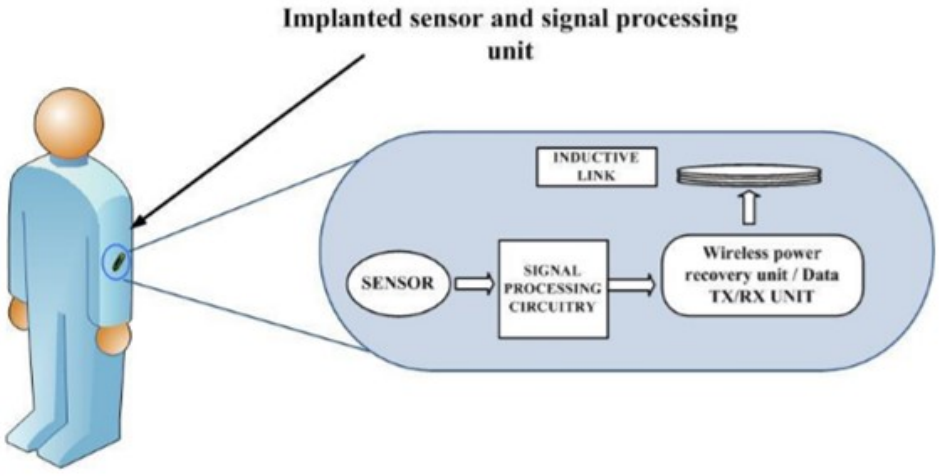


Figure 2: A minimally invasive glucose monitoring system [16].

Figure 3: Glucose sensing using contact lens [13].

1.3 Electrochemical Sensing Principle

Glucose sensing involves interaction with a family of biological catalyzer or enzymes. One such enzyme is Glucose oxidase. The basic concept of glucose biosensor is that GOx catalyzes the oxidation of β-D glucose by molecular oxygen producing H_2O_2 and gluconic acid. [1]

$$\text{Glucose} + \text{GOx} - \text{FAD}^{+} \rightarrow \text{Glucolacetone} + \text{GOx} - \text{FADH}_2$$

GOx needs a redox cofactor - FAD (Flavin adenine dinucleotide) which accepts electrons and gets reduced to $FADH_2$. The reduced enzyme loses two hydrogen atoms and combines with O_2 producing an H_2O_2 molecule.

$$FADH_2 + \text{Substrate} \rightarrow FAD + \text{Product}$$

$$FADH_2 + O_2 \rightarrow FAD + H_2O_2$$

There are other cofactors such as FMN- Flavin mononucleotide that works similarly to FAD. The final product of all these reactions is given below.

$$2H_2O_2 \rightarrow 2H_2O + O_2^+ + 4e^-$$

This reaction takes place by maintaining a constant difference potential at the electrochemical cell while collecting the electrons generated through a collector electrode. potentiostat provides the constant difference potential to be maintained at the electrochemical cell.

1.4 Types of Electrochemical Sensors

Electrochemical sensors are devices in which an analyte of interest reacts with the electrolyte producing an electrical signal which is proportional to the analyte concentration. A typical electrochemical sensor involves a working electrode and counter electrode separated by a thin layer of electrolyte. In a biosensor, the analyte of interest could be an enzyme, nucleic acid or hormone in a chemical solution or blood sample. Glucose sensing involves electrochemical sensors which are generally classified as potentiometric, conductometric, amperometric and voltammetric that detect the nature and concentration of the electrolyte.

1.4.1 Potentiometric Sensors

Potentiometric sensors measure the charge potential accumulated at the working electrode in an electrochemical cell in reference to the reference electrode when zero or no significant current flow between them. The linear response of the calibration curve is can be obtained using the Nernst equation. Interference from other ions and their long response time limit their usage in glucose sensing. One of the most commonly used potentiometric sensors is a pH meter.

1.4.2 Conductometric Sensors

Conductometric sensors measure the conductivity of the solution between two parallel electrodes in the presence of a given analyte concentration. It consists of a transducer to interpret the specific biological recognition as electric conductance. However, conductometric sensors are incapable of measuring solutions with lower concentrations and less accurate. They are less satisfactory when compared to other methods.

1.4.3 Amperometric and Voltammetric Sensors

Amperometric sensors operate by applying a desired potential to the electrochemical cell and produce a corresponding current (I_F) as a result of the redox reactions occurring at the working electrode. Current is measured only when the potential is applied. Whereas in voltammetric sensors, the applied potential at the working electrode is varied with respect to time and the resulting current is measured as a function of that potential. Amperometric sensors are widely used in the detection of glucose.

Amperometric sensors are divided into two electrodes and three electrodes system. Two electrodes system consists of a sensing electrode (WE) where the electrochemical reaction takes place and a reference electrode which is used for potential control and measurement. The current is measured through the working electrode, held at a fixed potential and RE is set to a constant potential. Three electrode system consists of another electrode called an auxiliary/counter electrode. In this case, the potential difference between RE and WE is maintained at a desired potential (E_i) irrespective of the electrochemical reaction taking place at WE. Current flows between CE and WE and no chemical reaction takes place at CE. WE is usually made of inert materials like Ag, Au, Pt, RE is made of Ag/AgCl and CE is made up of inert materials such as noble metal or graphite. Figure 4 shows the setup of two electrodes and three electrode system.

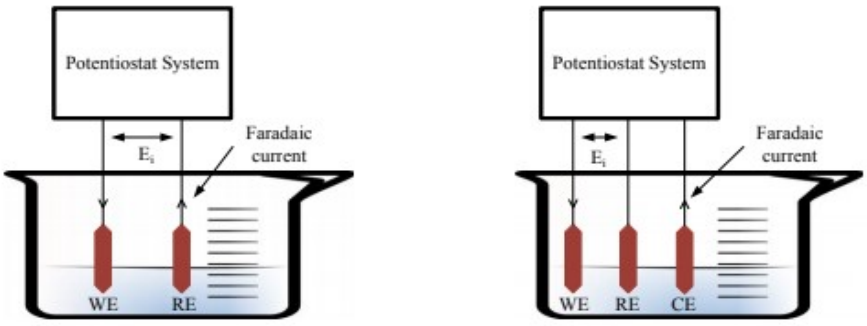


Figure 4: Two electrodes and three electrode system [19].

Two most widely used biosensors are O_2 based and H_2O_2 based sensors. In O_2 based sensors the cell potential is typically about 600mv, that is, the reference electrode should be at 600 mV higher than the working electrode. The sensor current flows from CE to WE. In H_2O_2based sensors, the oxidation of hydrogen peroxide at the surface of WE results in a sensor current which is proportional to the concentration of glucose. The cell potential is typically about 700mV, that is, the reference electrode should be kept at 700mv below the working electrode and the current flows from WE to CE. Figure 5 shows the current flow direction and the cell potential in O_2 based and H_2O_2 based sensors.

1.5 Research Goals

A potentiostat helps in providing a proper bias between the electrodes of a sensor. In other words, it enables the sensing system to measure a certain physiological element, as different physiological elements have different values of bias voltages.

The main focus was to develop low-voltage; low power potentiostat circuit with a wide sensor current range, high linearity and that could be incorporated in an implantable biosensor system. Importance was given to increasing the accuracy and reducing the mismatch in the circuit and improving the sensitivity in the measurement. Area constraints were also taken into consideration.

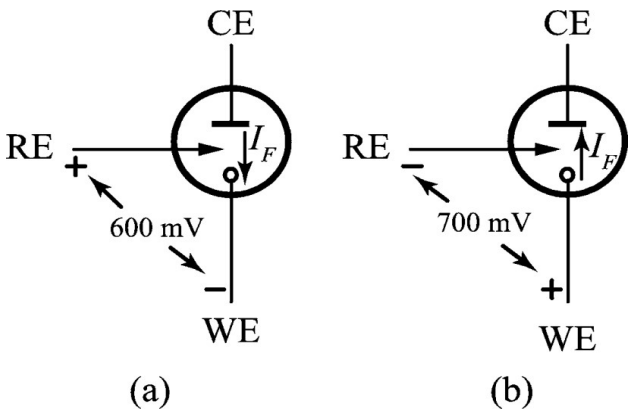


Figure 5: a) O_2 Based sensor b) H_2O_2 based sensor [14].

CHAPTER 2 - LITERATURE REVIEW

2.1 Principle of a Potentiostat

A potentiostat is an electronic device that maintains a constant potential between RE and WE and measures the current flow between the working electrode and counter (also called auxiliary) electrode and an integral part of glucose sensors.

There are three different potential configurations based on which electrode is held at the ground potential: grounded RE, grounded CE and grounded WE. Grounded RE and CE are considered to be the same from an electronic point of view. Among the two basic configurations, grounded WE is the most popular. As the name indicates, the working electrode is held at the ground potential and a control amplifier maintain the potential difference between RE and WE at a constant cell potential (E_i).

Grounded CE configuration was developed as an alternative. This configuration provides better protection by shielding WE against external electromagnetic interferences and ground noise but it involves more active and passive components which consumes more power and feedback loops. The grounded WE circuit topologies are widely used compared to grounded CE, which involves a single amplifier and consume less power, smaller area, and low noise.

2.2 Equivalent Models of an Electrochemical Cell

Different models have been used for modeling the electrochemical cell setup One of the models involve a parallel combination of a current source (I_{WE}) and a parasitic lumped R-C impedance [3] and another includes a combination of resistors and capacitors. In both the models, impedance is a combination of voltage-dependent polarized electrode junction capacitance and double layer parallel plate. Figure 6 represent equivalents model for the electrochemical cell.

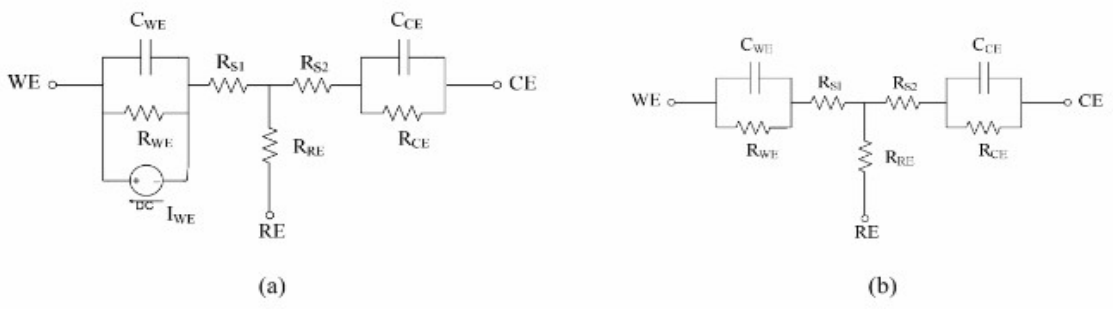


Figure 6: Two different equivalent models of an electrochemical cell [18].

R_{WE}, R_{CE}, and R_{RE} represent the resistance of working, counter and reference electrode respectively. C_{WE}, C_{CE}, C_{RE} represent the double layer capacitances of working, counter and reference electrode respectively. R_{S1} and R_{S2} represent the solution resistance. R_{WE} can be calculated by the equation below:

$$R_{WE} = \frac{E_i}{I_F} \tag{1}$$

Counter electrodes are smaller than working electrodes hence the resistance R_{WE} is much larger than R_{CE}. The solution resistances are much smaller compared to the counter electrode resistance and hence considered negligible.

2.3 Existing Potentiostat Configurations

2.3.1 Resistive Based Potentiostats

Figure 7shows the schematic of a transimpedance amplifier based potentiostat. It consists of a control amplifier and a TIA. The control amplifier uses the negative feedback to control the sensor current I_F, such that a fixed potential is maintained across the electrodes. The working electrode is at the virtual ground due to the negative feedback action of the TIA. The voltage across the feedback resistor is proportional to the sensor current. Smaller currents can be measured by increasing resistor to higher values without affecting the stability. The disadvantage of this circuit is that the input impedance of the TIA behaves inductively. The series connection

between TIA and CE, which has large capacitive components, contributes to the inductive behavior.

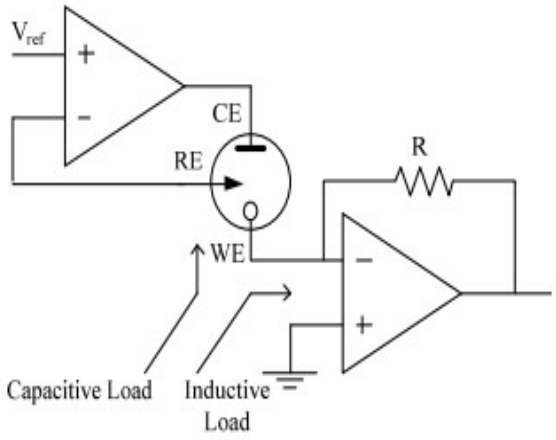


Figure 7: Transimpedence amplifier based potentiostat [18].

To address the issue of stability L. Busoni *et.al* [6] introduced a new structure as shown in Figure 8. The circuit employs grounded CE configuration rather than grounded WE configuration. The design employs TL018 opamps and other components. It is evident from the figure that the circuit is very complex and involves higher power consumption. This configuration is used in cases where shielding and screening of the working electrode connection from external electromagnetic interference (EMI) are difficult to implement, using a grounded-CE configuration may improve the current measurement

Another approach for measuring a current involves inserting a resistor in the current path of WE and measuring the voltage across the resistor which is shown in Figure 9. The advantage of this circuit is that WE is at ground potential but its potential changes. The measured potential is applied back to the control amplifier for proper potential control. But the circuit involves more active and passive components increasing the noise components consuming more power and area.

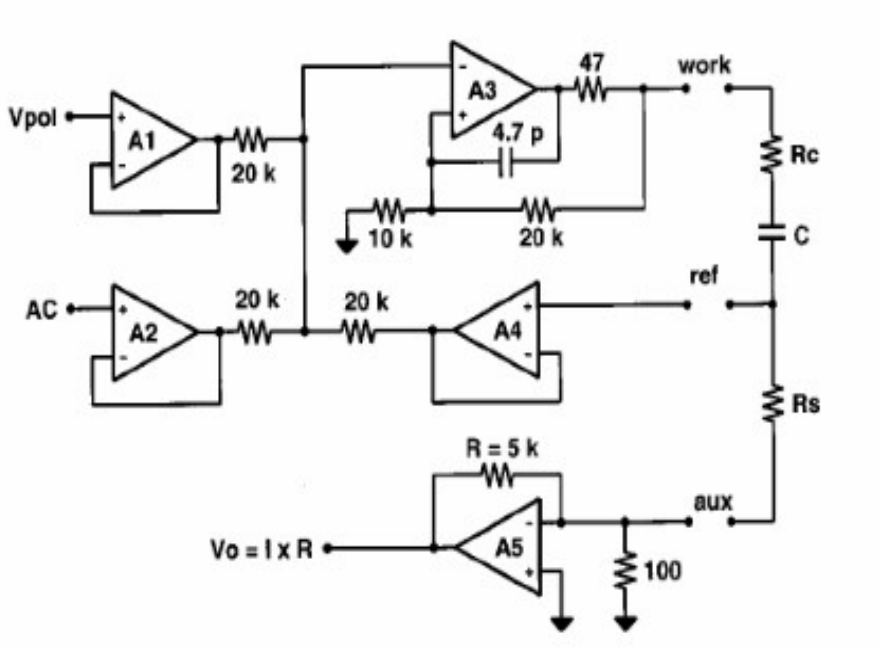


Figure 8: Grounded Auxiliary based potentiostat [6].

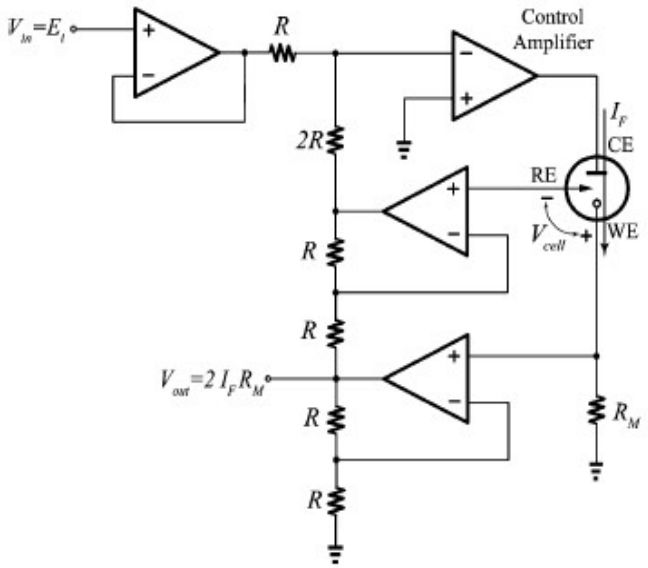
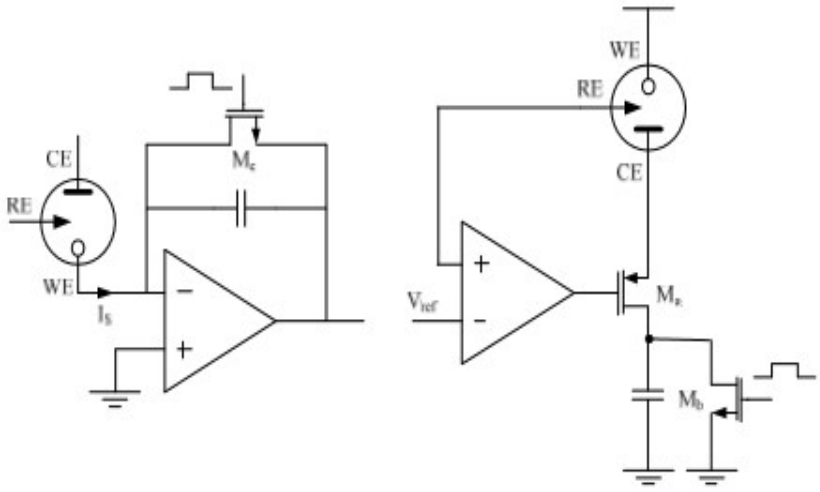


Figure 9: Potentiostat configuration with an inserted resistor at the WE current path [4].

2.3.2 Capacitive Based Potentiostat Configuration

The capacitive based approach is also called current conveyor approach is an alternative scheme to reduce the substantial chip area consumed by resistive based approach. It makes use of a capacitor that is charged and discharged by the sensor current. The circuit consists of a two electrodes system with the output sensor current directly connected to a capacitor that charges and discharges the capacitor, thus eliminating the current amplifying circuitry. Hence the circuit eliminates the matching problems and decreases power consumption and area and improves the dynamic range. For smaller currents, it does need a large value of capacitor unlike resistive approach which requires larger resistors. The current integration using a capacitor can be performed by either of the techniques shown in Figure 10.

An example that employs a capacitor for integrating the sensor current can be found in [5]. In this paper M. Breten *et al.* used Fig. 10(a) integrator to generate saw-tooth wave pulses by charging and discharging the capacitor.



(a) (b)

Figure 10: a) Current integration mostly used in current measurement using delta-sigma modulator. b) Current integration with a path of discharge which will be activated after capacitor reaches certain level of voltage [18].

This configuration is shown in Figure 11. In this configuration the sensor current (I_{mes}) charges the capacitor through switch S4 for time t_{up} and a constant DC current source (I_{ref}) discharges the capacitor through the switch S2 for time t_{down}.

The ratio of the charging time to the discharging time is proportional to the ratio of the sensor current to the current source current provided in this structure. This can be rewritten as:

$$I_{mes} = I_{ref} \times \frac{tdown}{tup} \tag{2}$$

Figure 12 represents another approach of current measurement using capacitive based potentiostat. The capacitor is charged to VDD through PMOS transistor and discharged through a NMOS transistor. The voltage across the capacitor is then compared with a reference voltage with the help of a comparator P1.

The other technique of integrating the current using a capacitor is shown Figure 13. The schematic comprises an additional transistor M2 to boost the output impedance. The integrating capacitor C_{int} is charged and discharged through the switch S2. The circuit introduces a pulse shaping circuit to fully discharge the integrator. By combining I-F converter and single slope ADC the circuit aims to achieve higher sample rate and improved dynamic range. [20]

Using integrator technique has a number of advantages over resistive based approach. Firstly, it needs less power and less chip area also it only needs one opamp. Secondly, the voltage across the opamp is not changing while the capacitor voltage is charging which helps to improve the stability and third; the opamp structure is not responsible for driving huge resistive load and hence reduces the output stage current requirement which leads to lower power consumption. The smaller currents can still charge the large capacitor by taking longer time which results in lower comparator output frequency and thus can be easily detected. However, the stability is still an important issue in these designs which is discussed in [22, 50].

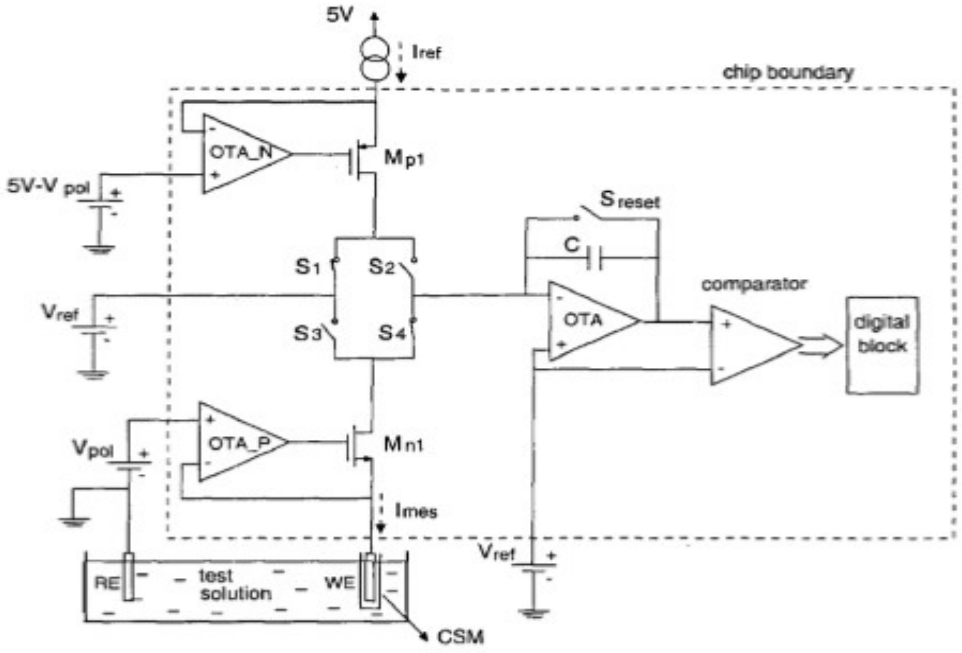


Figure 11: The current measurement technique according to M.Breten [5].

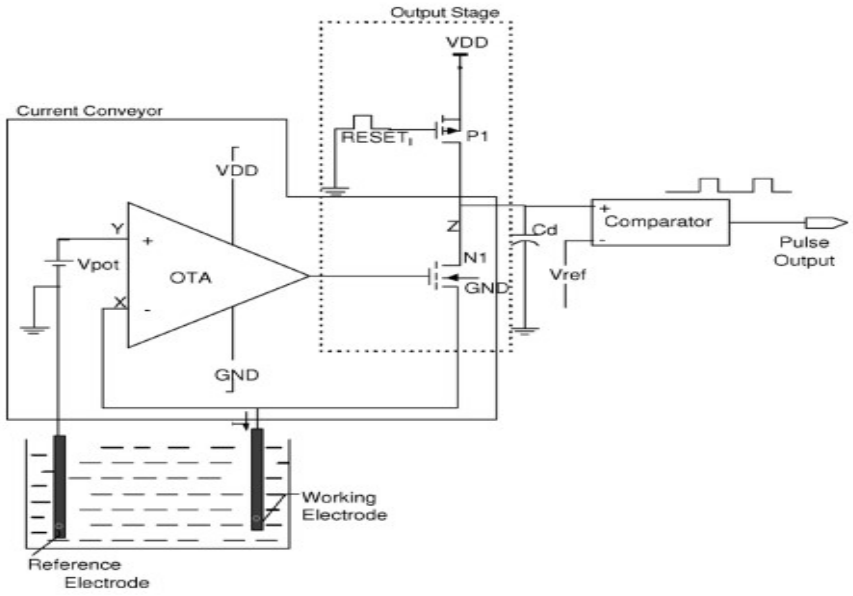


Figure 12: Capacitive based potentiostat diagram [9].

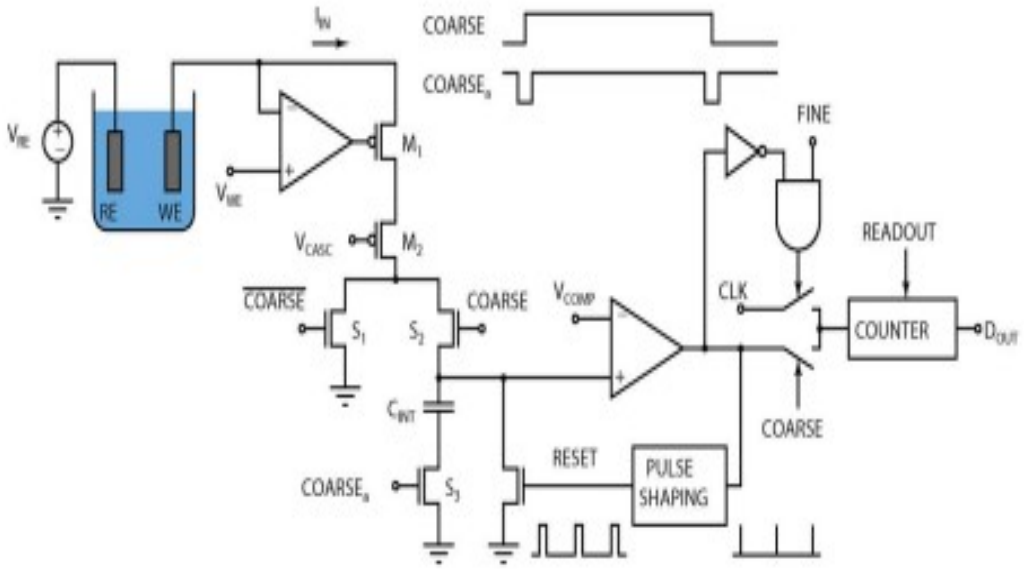


Figure 13: Schematic of single channel integrated potentiostat [20].

2.3.3 Current Mirror Based Potentiostat Configuration

This topology involves a current mirror circuit that generates a copy of the sensor current and processes the copied current than the sensor current itself. The circuit involves an opamp A_1 and a transistor M_1 in its feedback path which ensures RE and WE is maintained at V_{cell} potential. This circuit topology has many advantages over the aforementioned circuits. Firstly, WE is connected to true ground potential which reduces noise and interferences. Less active and passive components result in less power, noise and the circuit works well with single supply voltages. Figure 14 shows the basic schematic of the current mirror potentiostat.

However, this circuit still had stability issues. Figure 15 was introduced for increased stability which uses M_1 as a common drain stage instead of a common source stage. But the common drain stage introduces higher loop gain and hence it is more difficult to stabilize the potential control loop.

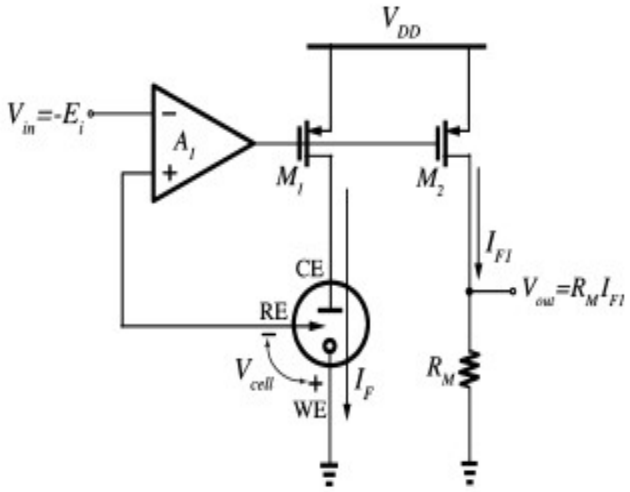


Figure 14: Schematic of the current mirror based potentiostat [14].

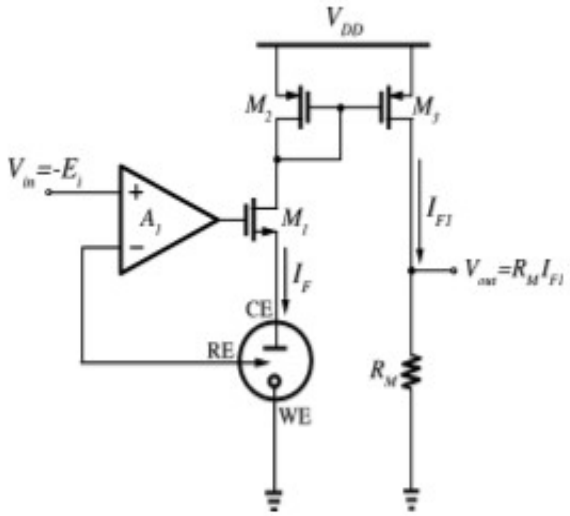


Figure 15: Schematic of the improved current mirror potentiostat [14].

It was noted from the conventional design as shown in Figure 16, the first pole was a varying pole and the second pole was a fixed which is an opamp pole that does not vary with the sensor current. To achieve higher stability, the second pole must be pushed to higher frequencies which require lower output resistance leading to lower open loop gain (A_O). M_1 should also be made smaller in order to decrease the g_{ma} and push P_1 to higher frequencies. The pole P1, P2 are given by the equations 3 and 4 respectively. Equation 5 represents the open loop gain of the opamp.

$$P_1 = -\frac{1}{C_{WE}((R_{WE}\|R_{ma})\|(\frac{1}{g_{ma}}))} \cong -\frac{g_{ma}}{C_{WE}} \tag{3}$$

$$P_2 = P_A = -\frac{1}{R_{out}C_{out}} \tag{4}$$

$$A_{OL} = -\frac{g_{ma}A_O(R_{WE}\|R_{ma})}{1+g_{ma}(R_{WE}\|R_{ma})} \tag{5}$$

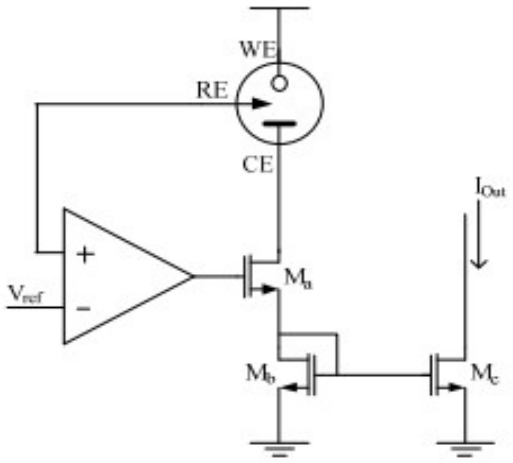


Figure 16: Improved current mirror circuit with a fixed first pole [18].

From the above equations, decreasing g_{ma} also results in decreasing open loop gain which results in higher offset and lowers accuracy. It is difficult to achieve higher open loop gain with good stability. Melika [18] introduced the circuit shown in Figure 16 to overcome the above problem. The Transistor M_1 was replaced by NMOS so the new structure had a fixed (non-variable) first pole. The new structure has two-stage amplifier without a compensation capacitor. However, the structure uses a NMOS as an amplifier rather than a common source which increases the loop gain and results in more unstable potential control loop. Also, the above configuration still suffers from systematic error due to channel length modulation and mismatch.

Starting the potentiostat involves moving the cell potential from zero to the potential V_{cell}, during which the impedance may vary considerably as the sensor highly depends on voltage during the startup. Hence the circuit may not be stable during the startup. Thus to over stabilize the circuit, an additional feedforward signal path was used to add the LHP zero to the potential control loop by M.M. Ahmadi *et.al* [14]. Figure 17 shows the schematic of the same.

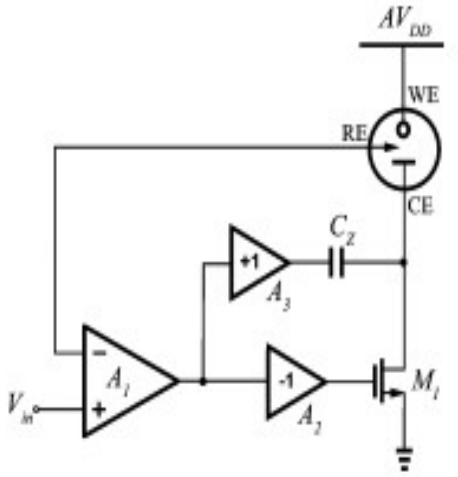


Figure 17: Improved current mirror potentiostat with added LHP zero [14].

2.3.4 Potentiostat Configurations with Improved Accuracy

To overcome the errors with the current mirror circuit and to increase the accuracy and reduce V_{DS} mismatch, the configuration shown below was introduced. This configuration consists of a potential control loop to maintain Vcell potential across WE and RE and an error control loop to improve the accuracy of the circuit. The circuit is as shown in Figure 18.

The error control loop consists of an error tracking amplifier and a transimpedance amplifier with adjustable input common mode voltage. Connecting OP_2 to common mode terminal of TIA introduces global feedback and enhances the loop gain of the error control loop. The V_{DS} mismatch between M_1 and M_2 after adding the error control loop was calculated and noted that $V_{DS\ (feedback)}$ causes offset error in the transfer function which could be eliminated by large loop gain of OP_2 and OP_3given by equation 6. However, this circuit involves more components and was not fabricated.

$$V_{out}= R_F I_{F1}-\Delta V_{DS(feedback)} \tag{6}$$

An alternate approach to improve accuracy and reduce power dissipation is as shown in Figure 19. This topology eliminates the need for auxiliary operational amplifier OP_2 thus reducing power consumption and uses a wide swing cascade mirror using M_1-M_4 instead. It uses negative feedback loops with operational amplifier A_1 and A_2 to achieve V_{DS} matching.

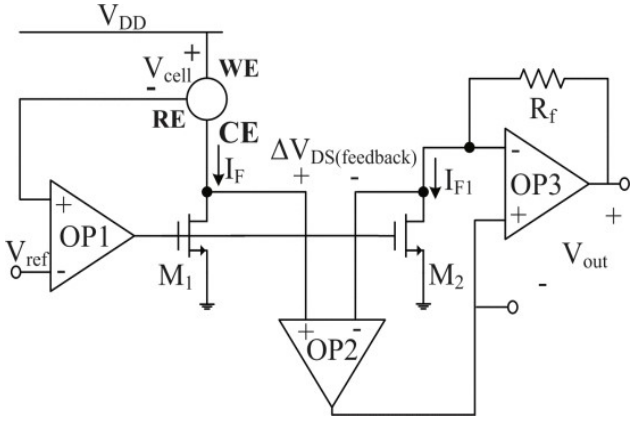


Figure 18: Current mirror potentiostat with error-cancellation loop for improved accuracy [17].

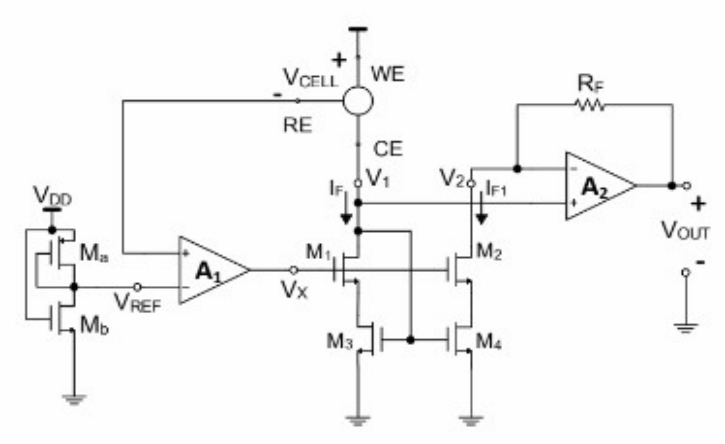


Figure 19: Low power potentiostat with improved accuracy [21].

2.3.5 Potentiostat Configurations with Improved Dynamic Range

Another circuit was introduced to provide a wide sensor current range, decrease the harmonics while detecting low-level current and provide wider dynamic range. The circuit consists of a potential control loop, current mirror structure, and a transimpedance amplifier. The circuit has a new interface compared to the transimpedance based potentiostat structure. Figure 20 and 21 show the schematic of single ended and fully differential potentiostat.

In this configuration, WE is at true GND potential and TIA is not connected to the potential control loop directly thus eliminating the chances of instability and oscillations due to the inductive behavior of the input resistance. Also, it reduces the limitation on saturated voltage and non-linearity issues seen in current mirror configurations.

The fully differential circuit is similar to the single ended structure except that the output voltage has a differential signal mode. It current mirror acts as a single to differential converter and produces two copies which produce two copies of current which are then converted to a differential voltage signal. It has double the amount of output swing compared to the single ended circuit and provides larger detectable current range and wider dynamic range. But the circuit needs a common-mode feedback circuit to control the common-mode voltage of the output signal.

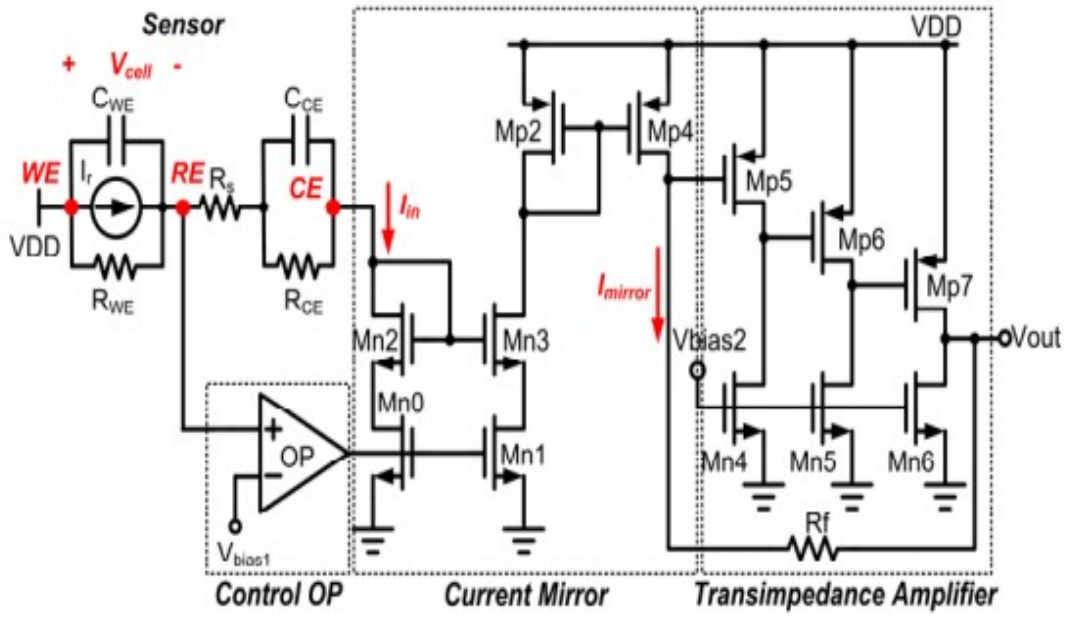


Figure 20: Single-ended potentiostat structure [15].

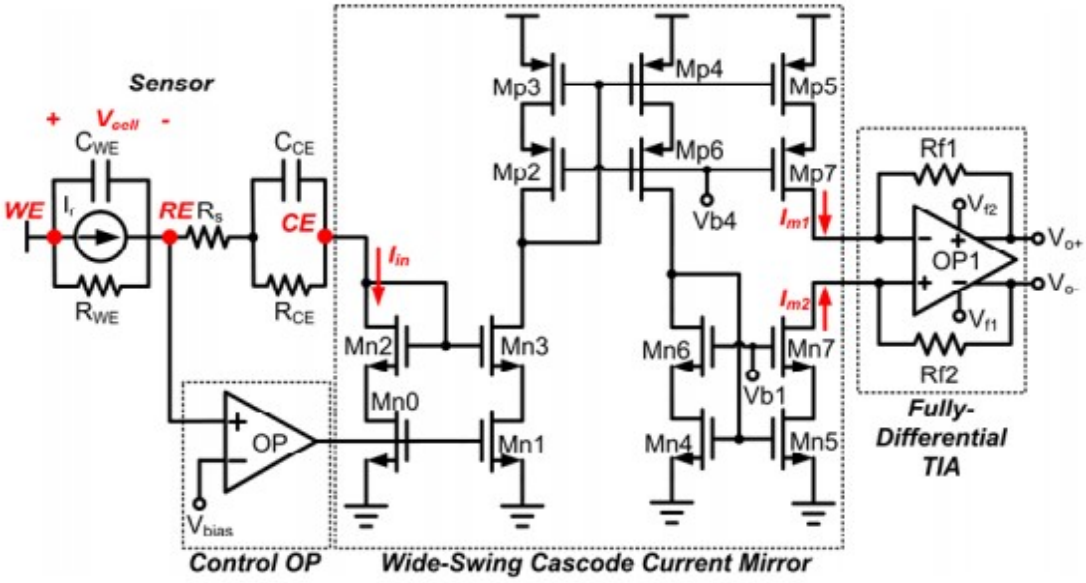


Figure 21: Fully differential potentiostat structure [15].

CHAPTER 3 - PROPOSED POTENTIOSTAT

As discussed in chapter 2, most of the potentiostat structures have stability and mismatch issues. This chapter presents an overview of the proposed potentiostat consisting of a control amplifier, current mirror, and a transimpedance amplifier. The block diagram of the potentiostat configuration is as shown in Figure 22. The control amplifier and transistor M_a constitute the control block that forms a potential control loop with the electrochemical cell to maintain the desired potential (V_{cell}) between WE and RE. The current mirror produces a copy of the sensor current and is fed to the amplifying part consisting of a tranimpedance amplifier which converts the current signal into a voltage signal output.

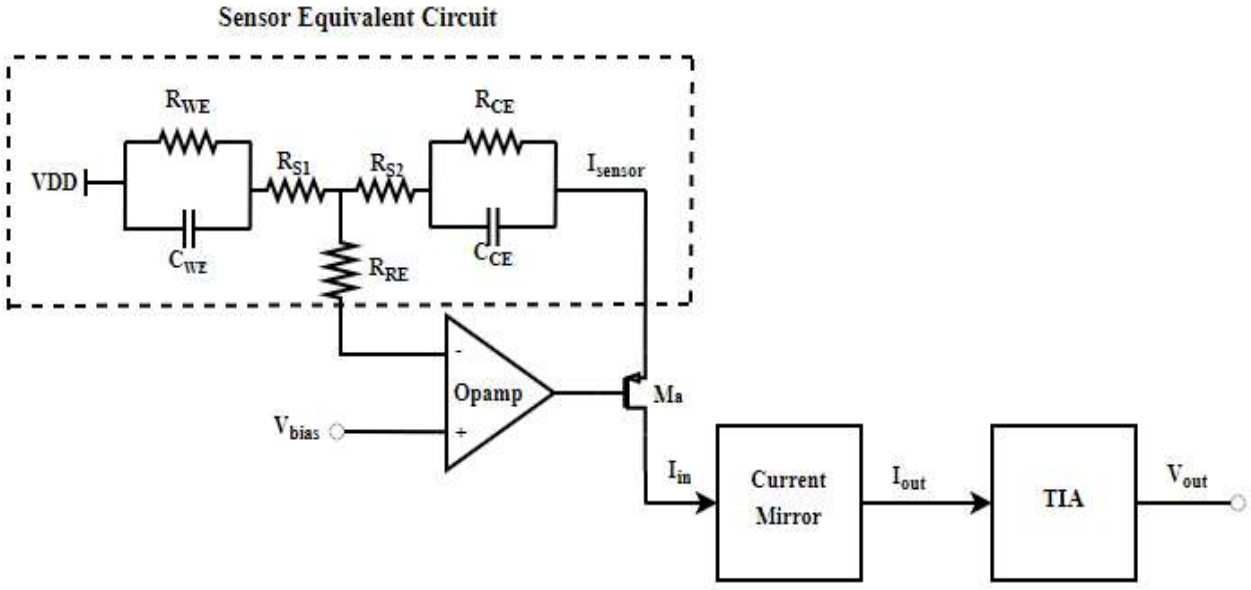


Figure 22: Block diagram of the proposed structure.

The main goal of the potentiostat is to maintain the desired potential across RE and WE and output the sensor current. The negative feedback action completed by opamp and transistor M_a maintains the potential across RE and WE to be at V_{cell} = 0.7V (considering H_2O_2 based sensor). A bias voltage, $V_{bias}= V_{DD}-V_{cell}$ is applied to the positive input of the opamp. The sensor current from equivalent circuit/electrochemical sensor will flow through transistor M_a into the current mirror and the mirrored current is fed to the TIA. The TIA provides a linear conversion of sensor current into voltage. The TIA is used as a single-ended structure with a feedback resistor. The feedback resistor can be switched to higher values to measure smaller currents. Note that the transimpedence amplifier stage is optional; the mirrored senor current from the V_{GS}-multiplier current mirror can be measured directly as the output. The equivalent electrochemical circuit in Figure 6 (b) has been used for simulation purpose.

The proposed structure has a number of advantages over the conventional structure. Using the above interface over resistive based potentiostat structures eliminates the possibility of the inductive behavior due to interface between TIA and potential control loop. Also, this interface avoids the large capacitive components contributed by the series connection between TIA and counter electrode. The proposed structure makes uses of a current mirror with V_{GS} multiplier biasing scheme [8]that eliminates the V_{DS} mismatch present in the conventional structures, is robust to temperature variations, and the sensitivity is considerably improved. The transimpedance amplifier linearly converts the sensor current into a voltage signal for readout.

The proposed structure is divided into 3 parts:

- Control Amplifier
- V_{GS}-Multiplier LVCCM Circuit
- Transimpedance Amplifier

3.1 Control Amplifier

The Control Amplifier topology is a current biased differential pair with bump degeneration and a folded cascode output stage. The schematic of the Control Amplifier is as shown in Figure 23.

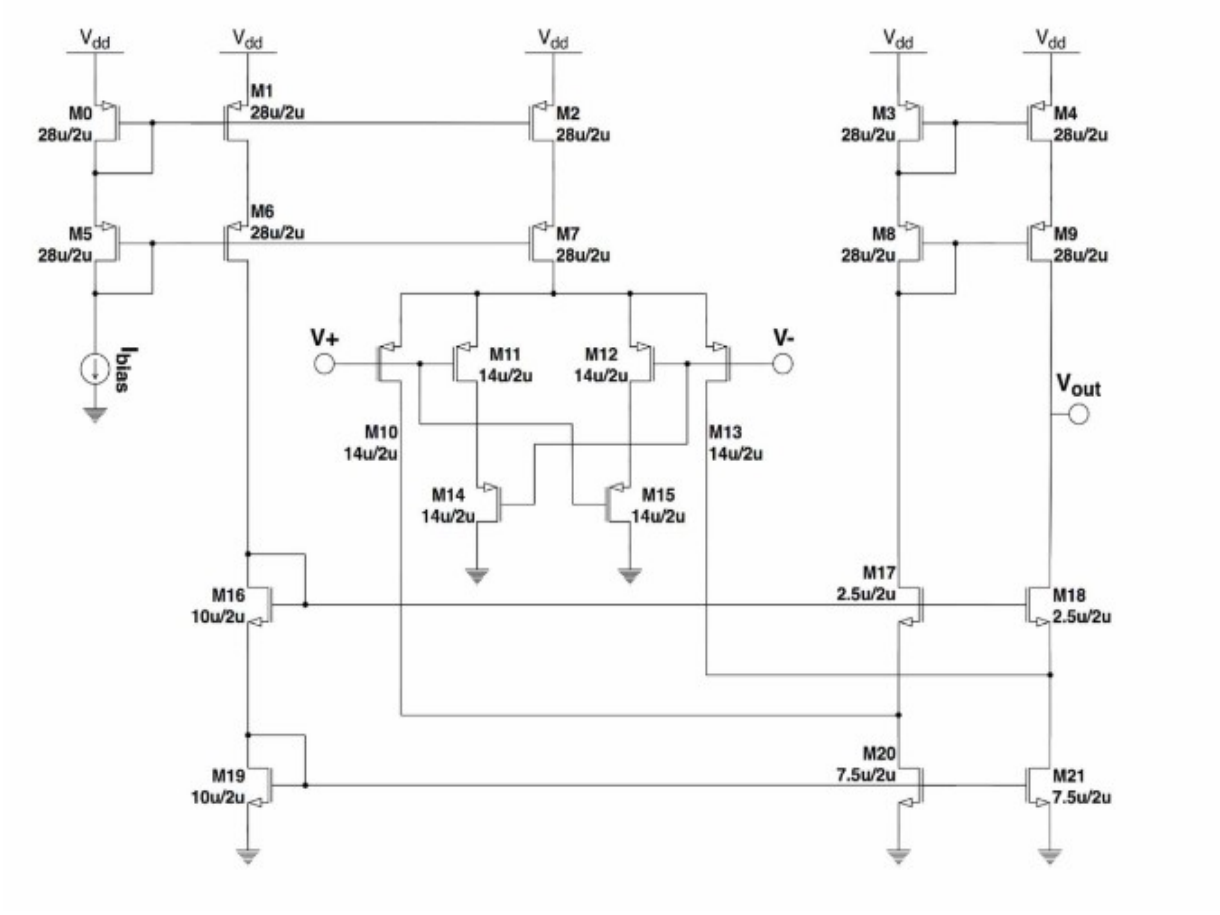


Figure 23: Schematic of the folded cascode control amplifier [28].

The control amplifier uses a four transistor bump degeneration that acts as degeneration resistors to provide wide linear differential input range. The cascode current mirrors are used to mirror the input bias current to the output biasing branch and source terminals of the PMOS differential input pair, the output of which is fed to the high output impedance folded cascode output stage [28].

The AC Equivalent circuit of the potentiostat is as shown in the Figure24. In the circuit below, C_{WE} is 1 µF, C_{RE} is 1 nF, R_{RE} is 6.3 kΩ, R_{S1} and R_{S2} are 10Ω, R_{CE} is 1 kΩ and R_{WE} varies from 25 kΩ to 25 GΩ depending on the solution concentration. R_{S1} and R_{S2} are very small compared to R_{CE} and R_{WE} and are neglected to simplify the equations. The amplifier is assumed to be a single pole structure with an open loop gain of A_0 and the pole is located at P_A.

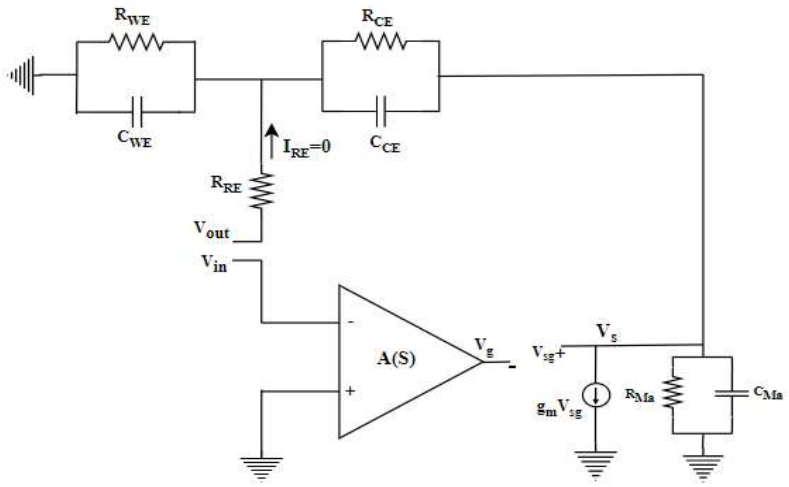


Figure 24: AC Equivalent circuit of the Potential control loop.

The transfer function of the control amplifier can be found in [18] which is given by equation 6:

$$\frac{\mathbf{Vout}}{\mathbf{Vin}} = \frac{-g_{ma}A_0}{1+{}^{8}/_{P_A}} \cdot \frac{1+R_{CE}C_{CE}s}{(1+g_A R_{CE}+R_{CE}C_{CE}s)\left(\frac{1+g_{ma}}{1+g_{ma}R_{CE}}+C_{WE}s\right)} \tag{6}$$

Based on the above equation, the transfer function has three poles and one zero whose location is given by equations 7, 8 and 9 respectively [18]:

$$P_1 = -\frac{1}{C_{WE}\frac{(R_{WE}\|R_{Ma})(1+g_{ma}R_{CE})}{1+g_{ma}(R_{WE}\|R_{MA})}} \tag{7}$$

$$P_2 = P_A = -\frac{1}{R_{out}C_{out}} \tag{8}$$

$$P_3 = -\frac{1+g_{ma}R_{CE}}{R_{CE}C_{CE}} \tag{9}$$

If g_{ma} and $R_{CE}$are designed to have a very small value, so that zero and the third pole (P_3) can cancel each other. By considering this assumption equation, the transfer function can be further simplified as to equation 10 shown below [18]:

$$\frac{\mathbf{Vout}}{\mathbf{Vin}} = \frac{-g_{ma}A_0}{1+{}^{s}/_{P_A}} \cdot \frac{(R_{WE}\|R_{Ma})}{(1+g_{ma}R_{WE}\|R_{Ma})+(R_{WE}\|R_{Ma})C_{WE}S)} \tag{10}$$

The transfer function now has two poles whose locations are given by equations 11 and 12 respectively [18]:

$$P_1 = -\frac{1}{C_{WE}((R_{WE}\|R_{Ma})\|(\frac{1}{g_{ma}}))} \cong -\frac{g_{ma}}{C_{WE}} \tag{11}$$

$$P_2 = P_A = -\frac{1}{R_{out}C_{out}} \tag{12}$$

From the above equations, it can be concluded that the dominant pole is generated by C_{WE} and $1/g_{ma}$, where g_{ma} varies with the sensor current. Thus the first dominant pole is variable one and the second pole is an opamp pole that is not affected by the sensor current. The size of transistor M_a was also carefully designed to push P_1 to lower frequencies and also the open loop gain of the control amplifier was considerably reduced.

3.1.1 Frequency Response

Figure 25 shows the Bode plot for 1 µA bias current with open loop gain of ~88 dB, a crossover frequency of 1.11 MHz and phase at the crossover frequency of ~90° and Figure 26 shows the bode plot for closed loop gain for 1 µA bias current, with the gain being unity until the cutoff frequency of 125 kHz is reached.

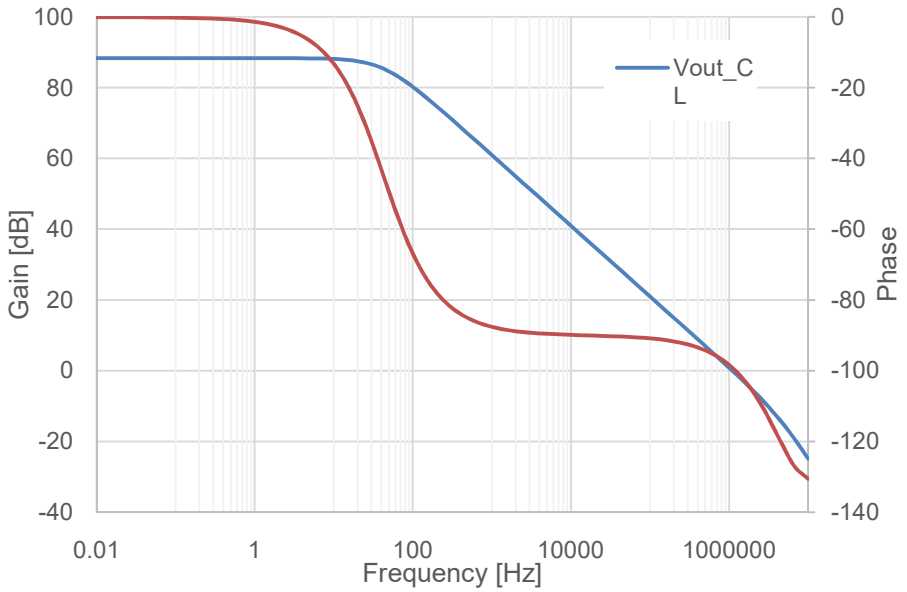


Figure 25: Control Amplifier open loop gain and phase for I_{bias} =1 µA.

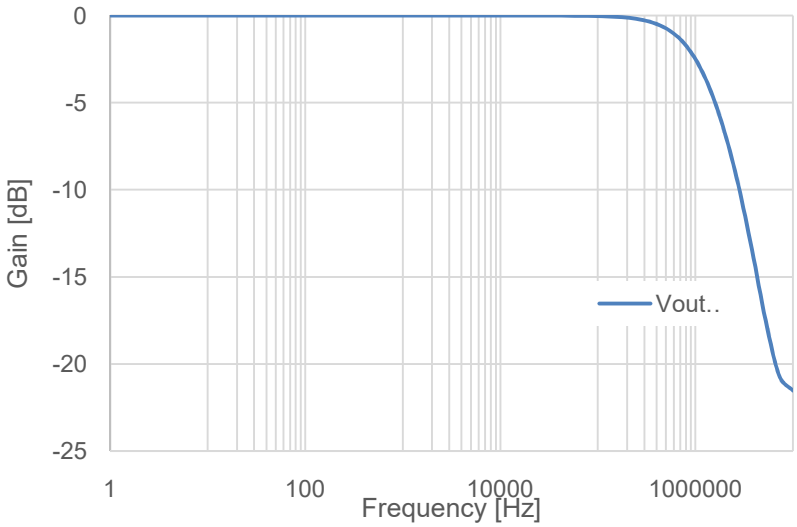


Figure 26: Unity gain plot for I_{bias}=1 µA.

3.1.2 Offset Simulation

The offset generated between the two inputs of the opamp was calculated using Monte Carlo analysis and mismatch simulation. The offset could be either due to the result of mismatch or due to the structure. The simulation result is as shown in Figure 27 that predicts a maximum mismatch of 20.77mV and is suitable for potentiostat application.

3.1.3 Common Mode Rejection Ratio

CMRR, the ratio of common mode gain to differential mode gain was calculated using the test setup shown in Figure 28. An ideal opamp will not respond to common mode signals. The CMRR was obtained using equation 13 shown below.

$$CMRR = 20\log\left(\frac{A_{DM}}{A_{CM}}\right) \tag{13}$$

The CMRR of this opamp is 56.21dB.

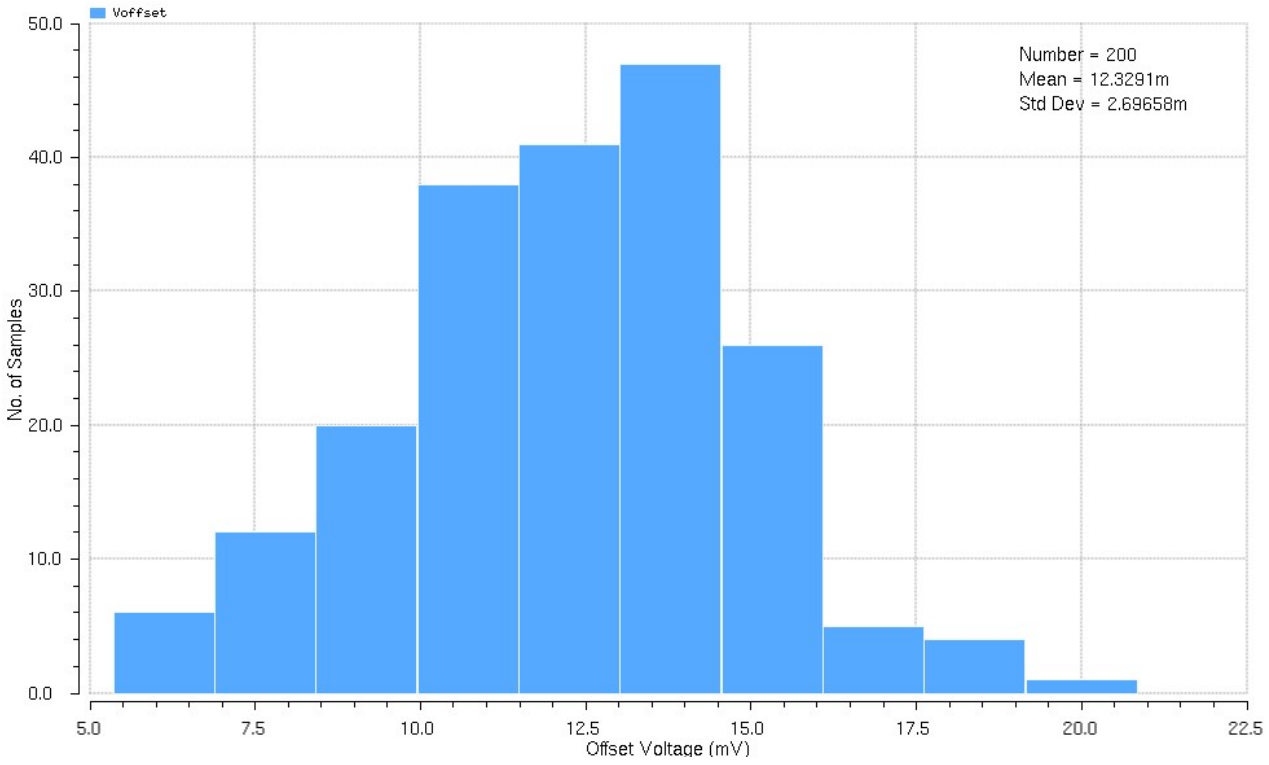


Figure 27: The offset between the two inputs of OTA.

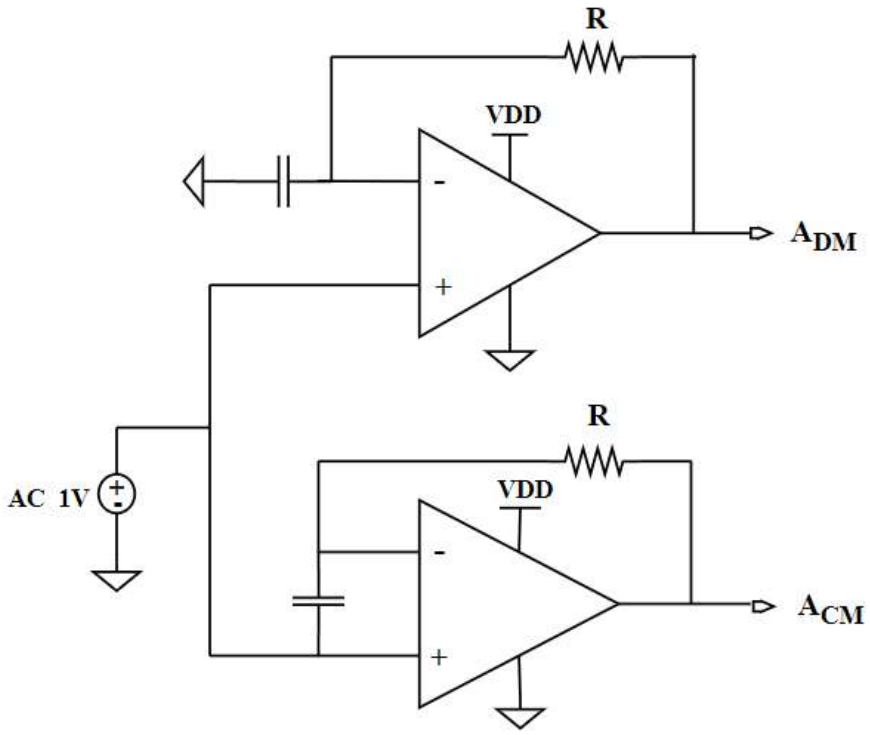


Figure 28: Circuit configuration for CMRR measurement.

3.1.4 ICMR of the Control Amplifier

Input Common mode range of an opamp is the range of common mode input voltage over which the amplifier behaves as a linear amplifier for differential input signals or input voltage range for which all the transistors operate in saturation. The test setup for ICMR simulation is as shown in Figure 29. The input voltage is varied from -1.8 V to 1.8 V and the resultant output voltage and the voltage at the tail current was noted. Figure 30 shows the simulated ICMR plot for the control amplifier. The input common mode voltage ranges from 0 to 1.4 V.

3.1.5 Performance Summary of the Control Amplifier

All the schematic simulation results of the control amplifier are summarized in this section. Table 1 shows the performance summary of the control amplifier. It was simulated in 0.18 μm process.

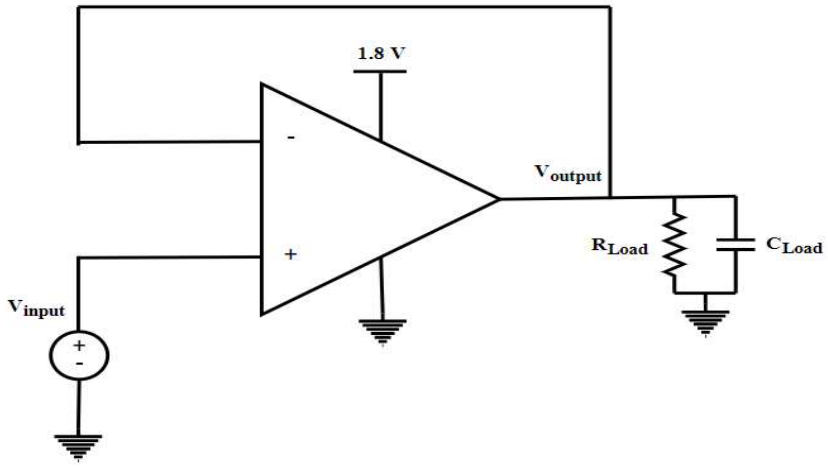


Figure 29: ICMR test setup.

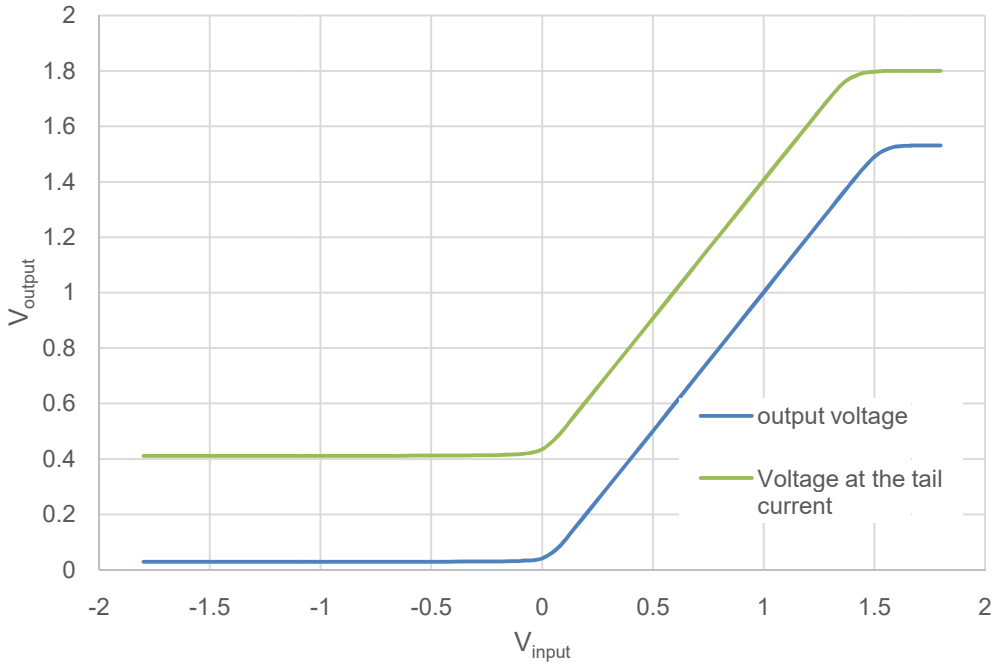


Figure 30: ICMR simulation of the control amplifier.

Table 1: Performance Summary of the Control Amplifier

Power Supply	1.8 V
Open loop gain	88 dB
Bandwidth	1.25 MHz
Phase Margin	89.9˚
Power Consumption	3.91 µW
Offset	12.32 mV
CMRR	56.21dB
ICMR	-106 mV to 1.56 V

3.2 V_{GS}-Multiplier Low Voltage Cascode Current Mirror

The main principle of the current mirror is to mirror the sensor current into another circuit and process the copied current instead of the sensor current itself. A number of Current mirror based potentiostat configurations have been reported in the literature [14][18][15][16]. All of these approaches suffer from systematic errors due to channel length modulation of M_1 and M_2 and random errors such as device mismatch, V_{DS} mismatch, and temperature variations. The random errors can be calibrated out from potentiostat response; however, there remains a calibration error which might degrade the accuracy. The current mirror approach reported in [17] eliminates the systematic error. However, the topology still suffers from random errors and the circuit was only simulated and not fabricated. Current mirror with Minch bias scheme [7] was also taken into consideration, the Minch current mirror device uses low voltage cascode current mirror circuitthat is biased at the edge of saturation which compromises the output impedance. For high output impedance current sources and current references, this is not acceptable.

The V_{GS}-multiplier based LVCCM topology eliminates the random errors such as V_{DS} mismatch and temperature vulnerability in the current mirror based potentiostat. The V_{GS} multiplier techniques provide guaranteed saturation operation overall temperatures but it also

provides some voltage headroom so that output impedance can be improved. The working of the V_{GS} Multiplier LVCCM is as follows. The opamp senses the V_{GS} of M_1that is used as the opamp input and produces an output of $1.5V_{GS}$. This output voltage is used to bias the gates of the cascode transistors. Neglecting the body effect, assuming all the devices are matched, the V_{DS} on all the transistors are matched to $0.5V_{GS}$ independent of operating region (weak, moderate or strong inversion saturation) and temperature [8]. Thus the characteristic of the V_{GS} multiplier is that the V_{DS} of M_1, M_2 and M_4 transistors are matched thus eliminating V_{DS} mismatch and temperature sensitivity. The opamp used in the V_{GS}-multiplier mirror is a two stage opamp that is briefed in Transimpedence Amplifier section. Figure 31 shows the schematic of the V_{GS} multiplier low voltage cascode current mirror.

Table 2 shows the transistor aspect ratio of the current mirror circuit. The current mirror opamp was biased with 1 µA bias current. The circuit was simulated for closed loop gain and phase and for temperature variations using 10 kΩ resistors. Monte Carlo analysis was performed to simulate the matching requirements. The simulation results are provided in the sections below.

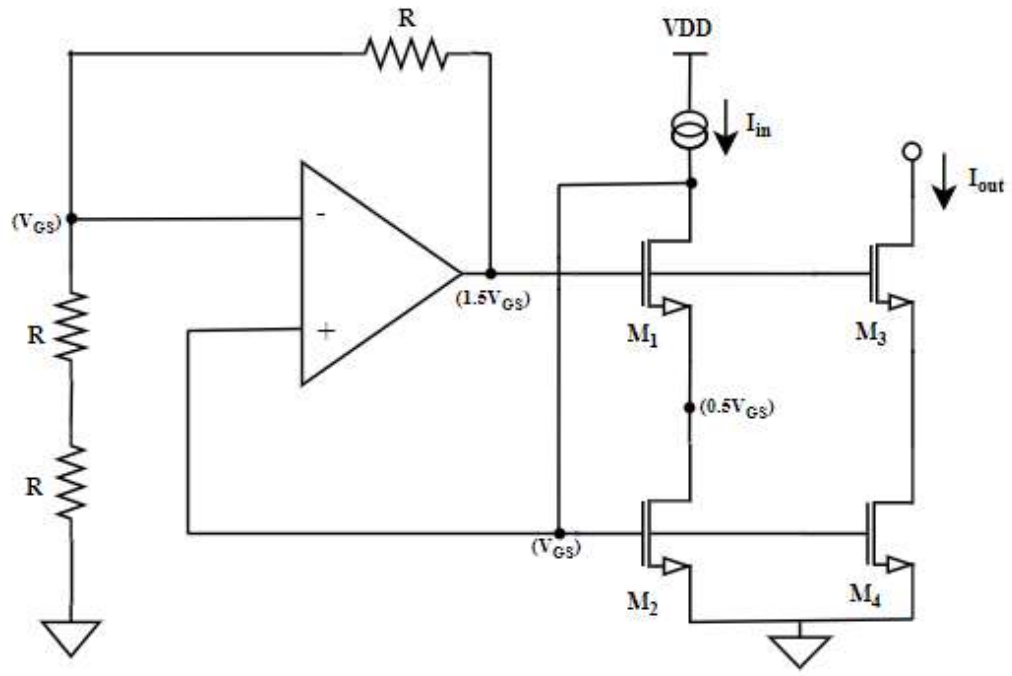


Figure 31: V_{GS}-multiplier Low voltage cascode current mirror.

Table 2: Transistor Aspect Ratio of the V_{GS}-Multiplier LVCCM

Transistor	W/L (µm / µm)	Transistor	W/L (µm / µm)
M1	5/2	**M3**	5/2
M2	5/2	**M4**	5/2

3.2.1 Feedback Stability

Stability analysis was performed to calculate the closed loop gain and phase of the feedback loop in the current mirror. Figure 32 shows the Bode plot with a closed loop gain of ~40 dB and a crossover frequency of 2.47 MHz and phase at the cross over frequency is ~95° for a bias current of 1 µA.

3.2.2 Matching Requirements

The current mirror requires very good matching in order to accurately create a copy of the sensor current. Mismatch is usually due to systematic and random errors such as device mismatch, V_{DS} mismatch. Much was taken in the layout block of the Current Mirror. The opamp within the current mirror was designed using common centroid techniques that reduce process mismatch significantly in both X-axis and Y-axis.

Monte Carlo simulations were performed for process variation and mismatch in V_{GS}-multiplier current mirror for different values of sensor current that clearly demonstrated their expected benefit. Table 3 summarizes the Monte Carlo analysis results. Figure 33 shows the Histogram for 10 nA sensor current. It is evident that the current mirror has a linear range of operation over a very wide range from 100 pA to 100 µA.

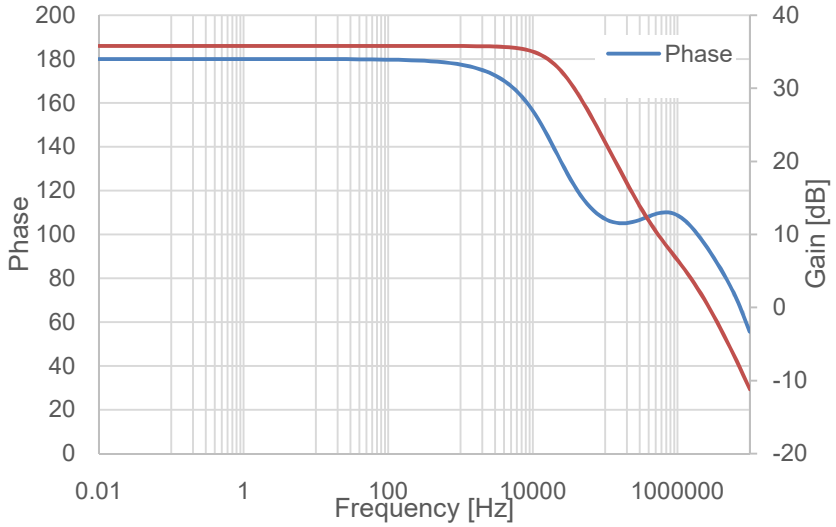


Figure 32: Closed loop gain and phase for I_{bias}=1 µA.

Table 3: Monte Carlo Simulation Characteristics for Output Current of the V_{GS} LVCCM

I_{out} (A)	Min (A)	Max (A)	Mean (A)	Std Dev	%Mismatch
100 µ	98.56 µ	100.9 µ	99.97 µ	450 n	0.0045%
10 µ	9.665 µ	10.23 µ	9.998 µ	116.2 n	0.0116%
1 µ	945.3 n	1.039 µ	999.7 µ	19.89 n	0.0198%
100 n	93.57 n	104.7 n	99.98 n	2.401 n	0.024%
10 n	9.314 n	10.51 n	9.999 n	260.9 p	0.026%
1 n	931.4 p	1.053 n	1.001 n	27.02 p	0.027%
100 p	100.3 p	109.7 p	102 p	1.833 p	0.0183%

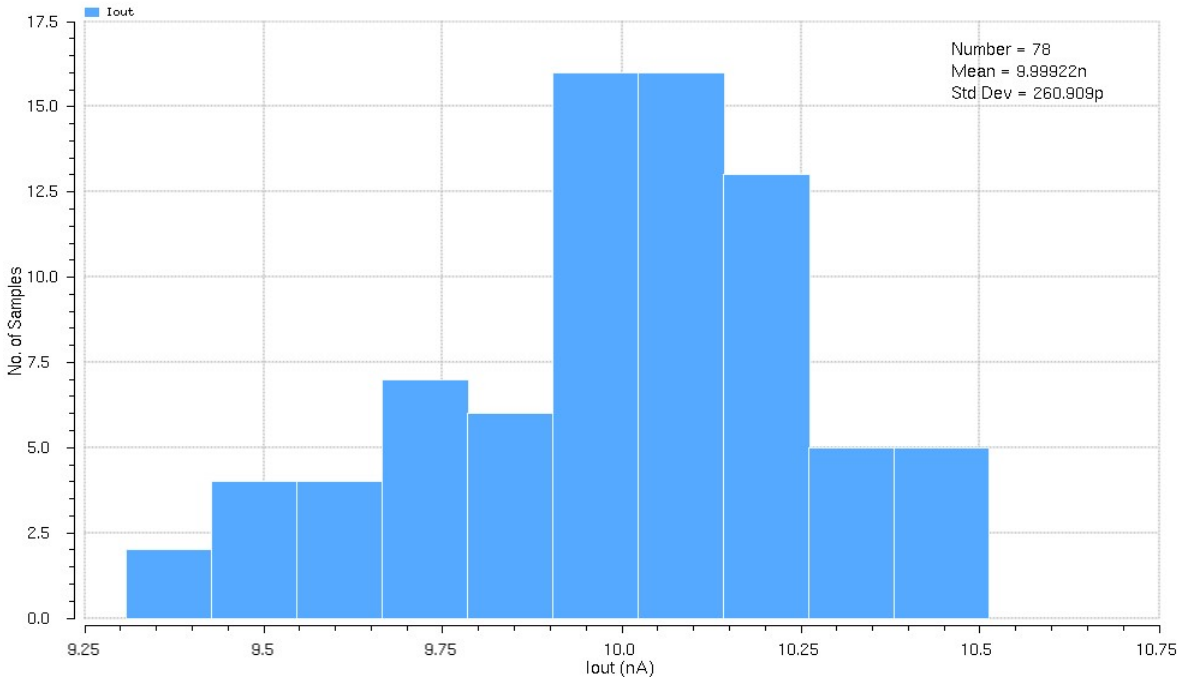


Figure 33: Monte Carlo analysis of process variation and mismatch effect in V_{GS}-multiplier Current Mirror.

3.2.3 Temperature Variations

The V_{GS}-multiplier current mirror circuit guarantees saturation operation over all temperature. The circuit was simulated for a temperature range of -100°C to 50°C in steps of 50°C. Figure 34 represents the simulation of the I_{OUT} versus V_{OUT} characteristics for a LVCCM biased with a V_{GS}-multiplier. One can clearly see that all the devices in the mirror remain in saturation over this large range of temperatures, as evident from the fact that I_{OUT} remains virtually constant for V_{OUT}> 0.4 V. Since there is minimal temperature sensitivity in the current mirror it would be ideal incorporate in an implantable sensor as it would sustain variations in body temperature and giving nominal performance.

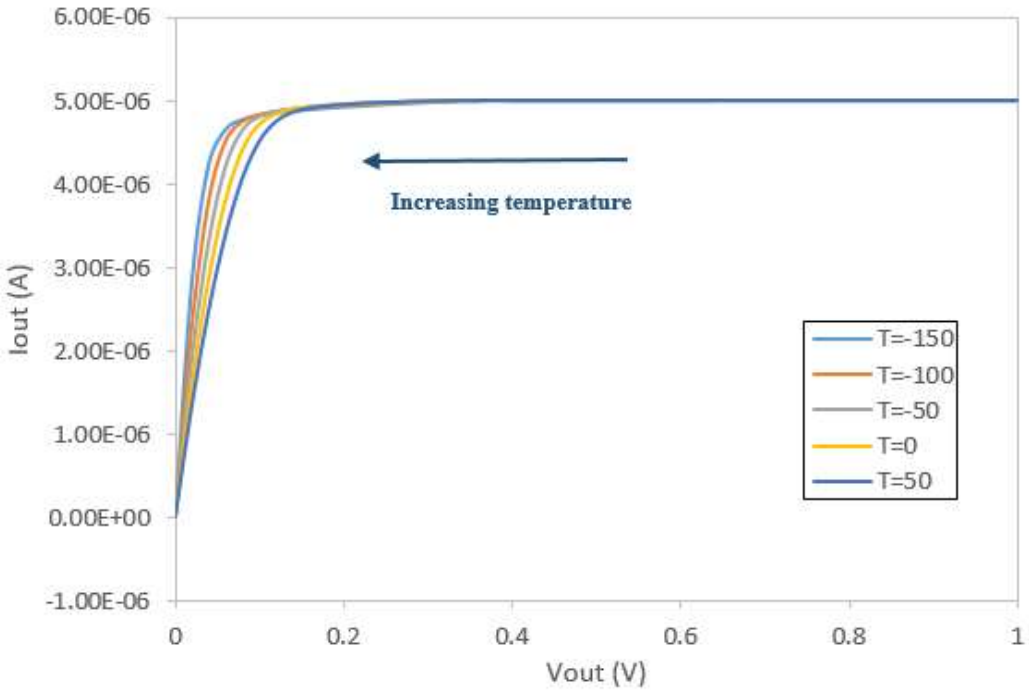


Figure 34: Simulated I_{out}-V_{out} for V_{GS}-multiplier LVCCM for different temperatures.

3.3 Transimpedance Amplifier

The transimpedence amplifier uses a two stage cpamp for linear conversion of sensor current into voltage. The TIA has a current biased pmos input differential pair with a Class AB output stage that is Miller compensated. It produces a single-ended output. The same opamp schematic has been used for the opamp in V_{GS}-multiplier current mirror block. Figure 35 represents the detailed schematic of the opamp. It was also used to obtain the voltage regulation of the current mirror. The TIA is used in an inverting configuration with feedback resistor R_F in the potentiostat circuit.

Figure 36 shows the TIA setup for the feedback factor calculations. The circuit is compensated by a feedback capacitor C_F. From this circuit, it is easy to derive the transfer function of the transimpedance amplifier.

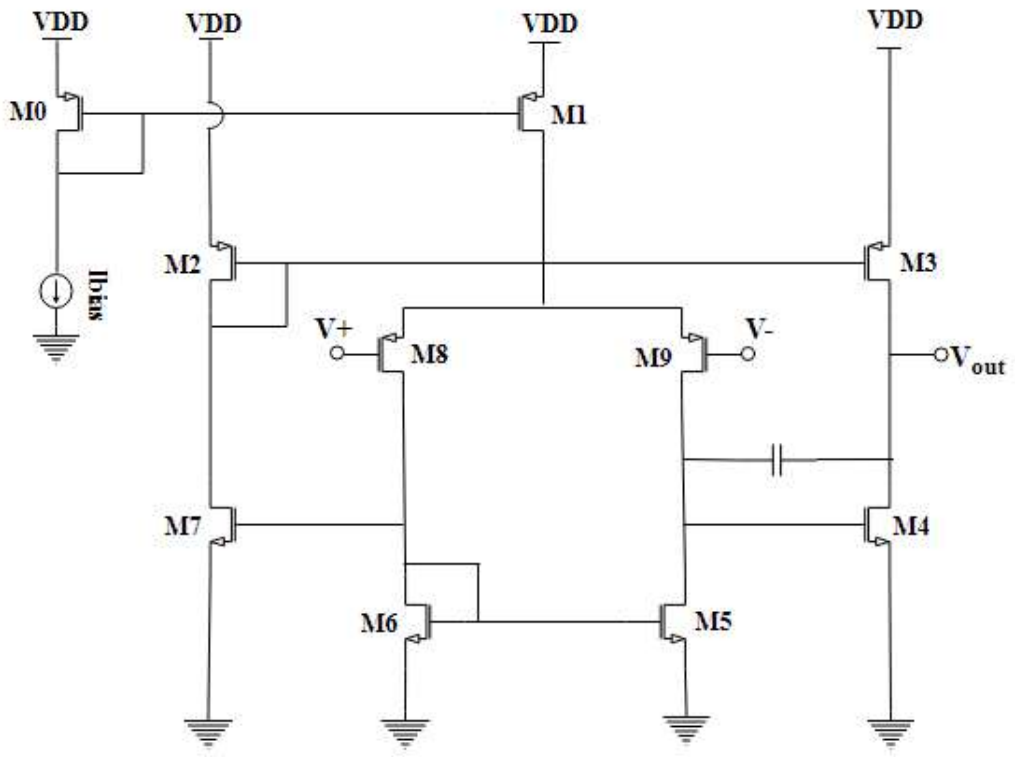


Figure 35: Schematic of the opamp for Transimpedence amplifier [28].

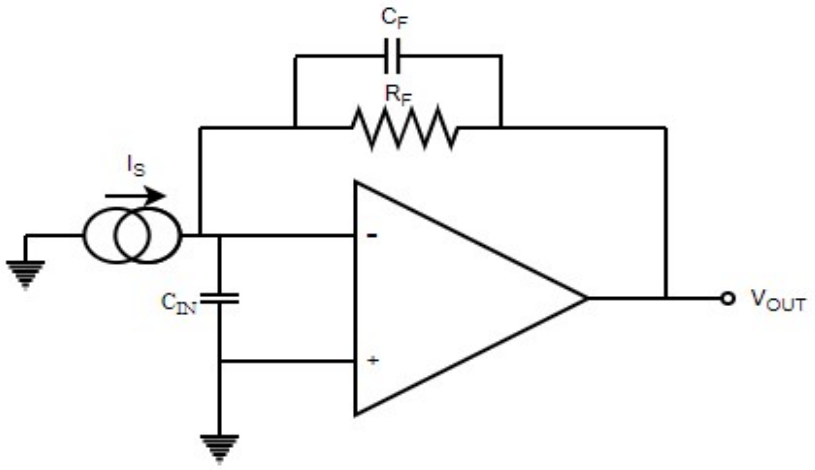


Figure 36: AC Equivalent circuit of TIA.

The opamp is assumed to be ideal; therefore, the inverting input is at virtual ground. The opamp is a voltage amplifier, not a current amplifier. The current source (I_S) has infinite impedance; therefore, it has no effect on the feedback factor.

The two input capacitors are combined by setting $C_{IN}=C_J+C_{CM,}$ where C_J is the junction capacitance and C_{CM} is the common mode capacitance. They have no effect on the transfer function of this circuit since both nodes are at AC ground.

The transfer function for the transimpedance amplifier is given the equation 13:

$$F=\frac{1+sC_FR_F}{1+s(C_{IN}+C_F)R_F} \tag{13}$$

It has one zero and one pole whose location is given by the equations 14 and 15 respectively:

$$f_Z=\frac{1}{2\Pi(C_{IN}+C_F)R_F} \tag{14}$$

$$f_Z=\frac{1}{2\Pi C_FR_F} \tag{15}$$

3.3.1 Frequency Response

The opamp open loop simulations were conducted with 1 μA bias with 10 MΩ and 15 pF load in unity gain configuration. Figure 37 shows the Bode plot with an open loop gain of 73.77 dB, a crossover frequency of 2.68 kHz and phase at the crossover frequency of ~114°. Figure 38 shows the bode plot for closed loop gain with the gain being unity until the cutoff frequency of ~23 kHz.

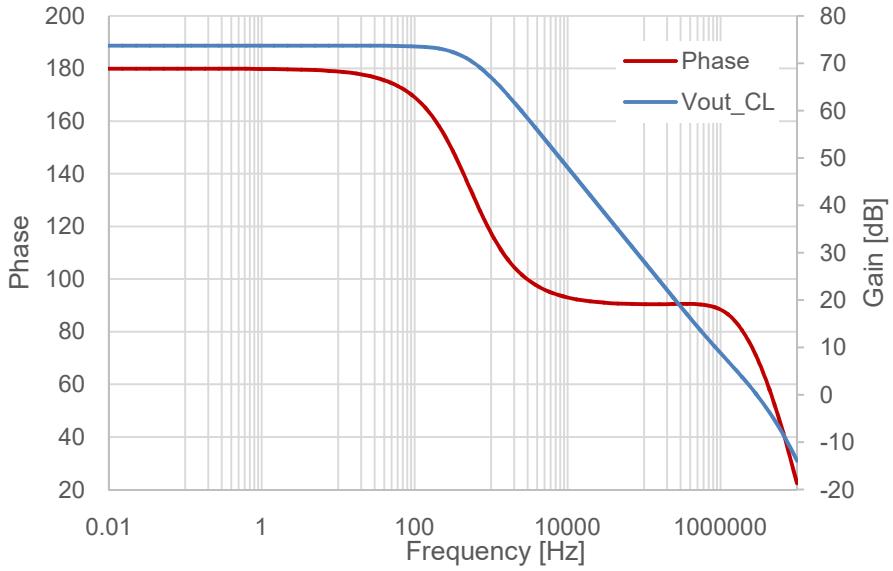


Figure 37: Opamp Open loop gain and phase for I_{bias}=1 µA.

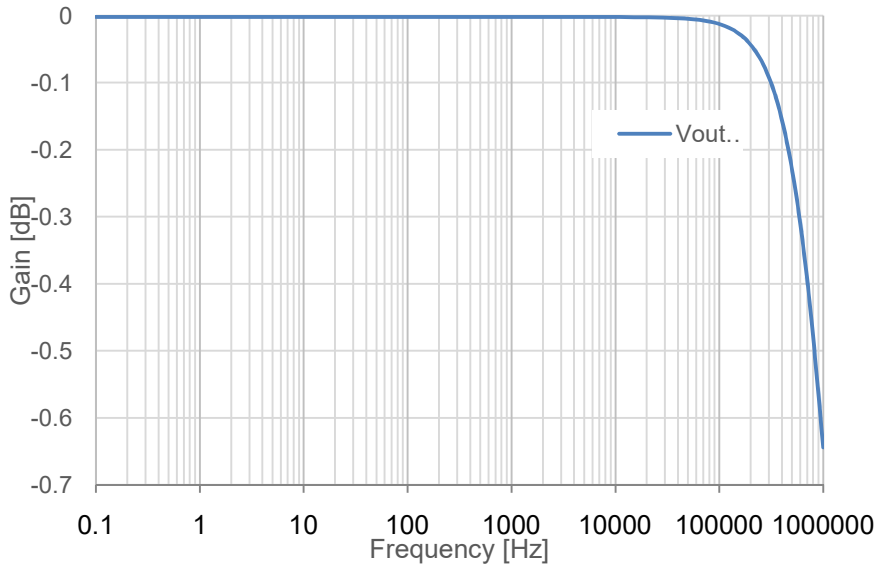


Figure 38: Opamp unity gain plot for I_{bias}=1 µA.

3.3.2 Offset Simulation

The offset between the two inputs of the TIA was calculated using Monte Carlo analysis variation and mismatch analysis. Figure 39 shows the Monte Carlo simulation results and has the worst-case mismatch of 7.577 mV.

3.3.3 Common Mode Rejection Ratio

The common mode rejection ratio of the TIA was simulated using the same setup as in Figure 28. The resultant CMRR for the TIA was 77.45 dB.

3.3.4 ICMR

The ICMR of TIA was simulated using the same setup as shown in section 3.1.4, used for the ICMR measurement of OTA. Figure 40 shows the ICMR plot of the opamp. The opamp has an ICMR of 0.1 V to 1.4 V.

3.3.5 Performance Summary of the TIA

All the schematic simulation results of the transimpedance amplifier are summarized in this section. Table 4 shows the performance summary of the TIA that was simulated in 0.18 µm process.

Table 4: Performance Summary of the TIA

Power Supply	1.8 V
Open loop gain	74 dB
Bandwidth	2.5 MHz
Phase Margin	66˚ (R_F=10 kΩ)
Power Consumption	334 µW
Offset	130µV
CMRR	77dB
ICMR	0 to 1.4 V

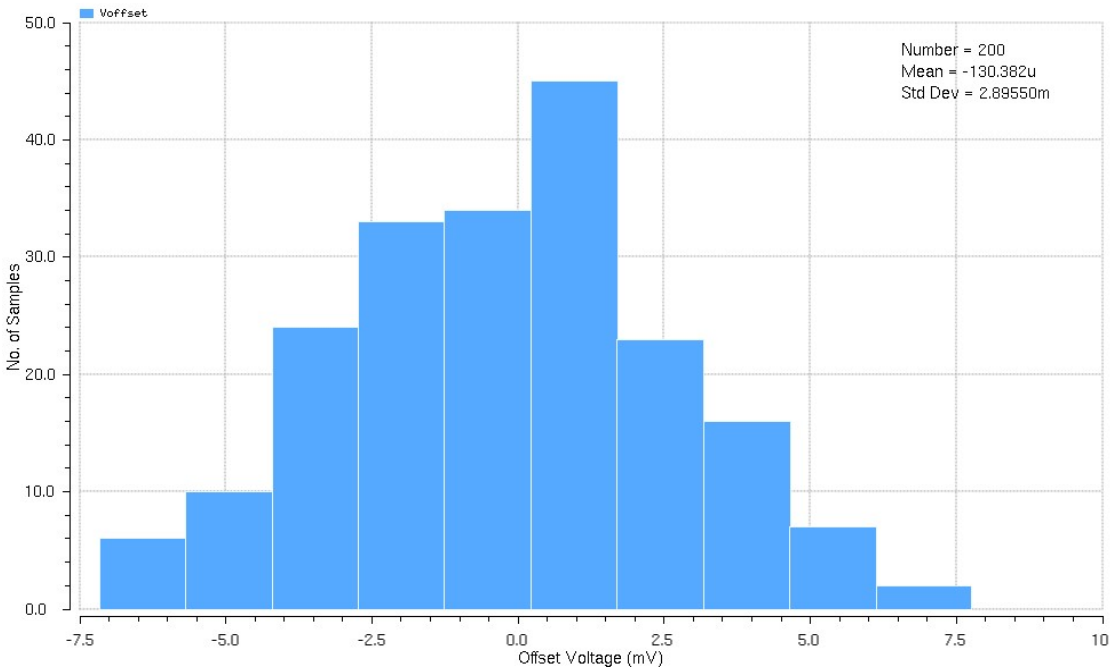


Figure 39: The offset between the two inputs of TIA.

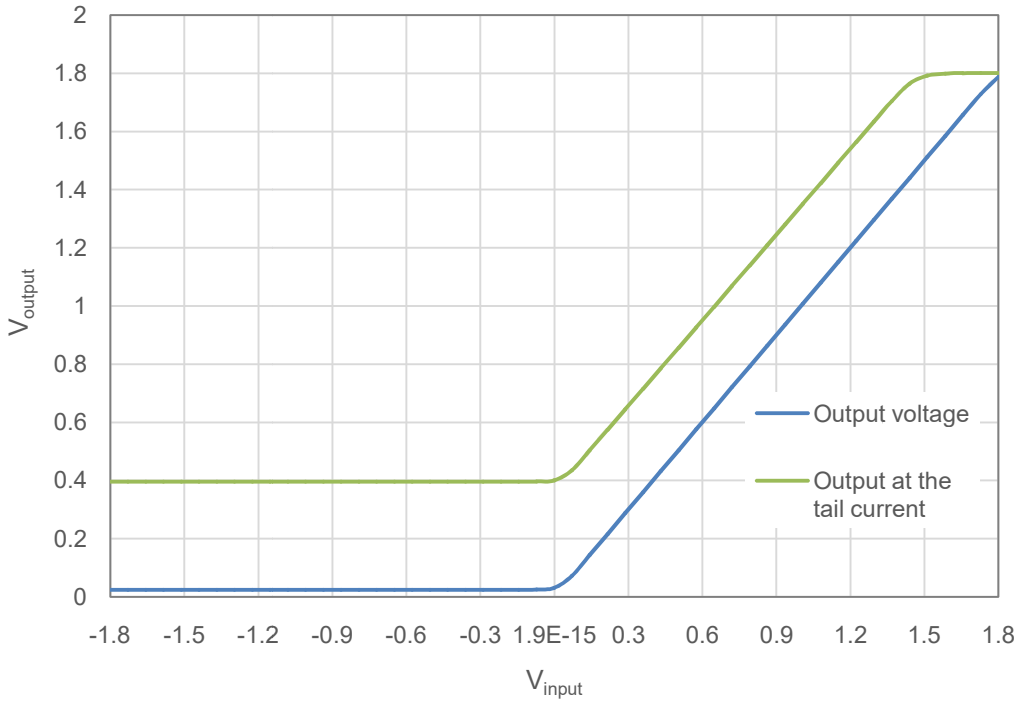


Figure 40: ICMR simulation of TIA.

3.4 Performance of the Potentiostat

The design was simulated with varying V_{cell} voltages to analyze the range of voltages for which the potential control loop is stable. The design operates with desired characteristics for a V_{cell} voltage range of 0.3 V to 1.3V and hence the potentiostat can be used for various electrochemical sensing applications which require a V_{cell} within the range mentioned.

3.4.1 Electrode Voltages

As discussed earlier, one of the main principles of a potentiostat is to maintain a constant potential between the working and reference electrode. Considering H_2O_2based glucose biosensor, the difference between the reference electrode and working electrode should be 0.7 V for varying working electrode resistance. The resistance is used to indicate the solution resistance in which electrodes are immersed. Figure 41 shows the voltage across working and reference electrodes for varying resistance from 25 kΩ to 25 GΩ. Figure 42 shows the difference in potentials across electrodes for varying resistance. The X-axis represents varying analyte concentration. Y-axis represents the difference in voltage across WE and RE which starts with 0.697Vfor 25 kΩ to settles to 0.7 V as the resistance increases.

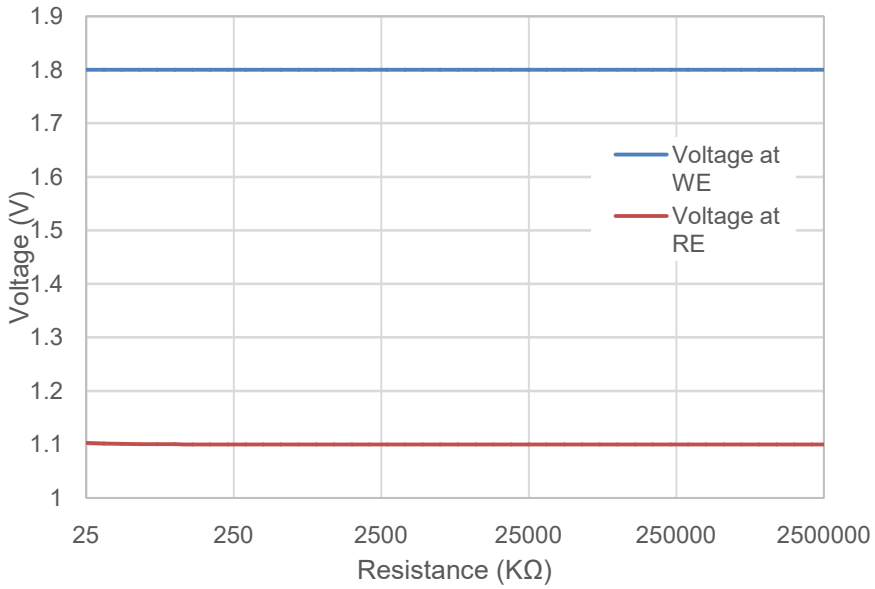


Figure 41: Voltages at the working electrode and reference electrode versus $R_{WE.}$

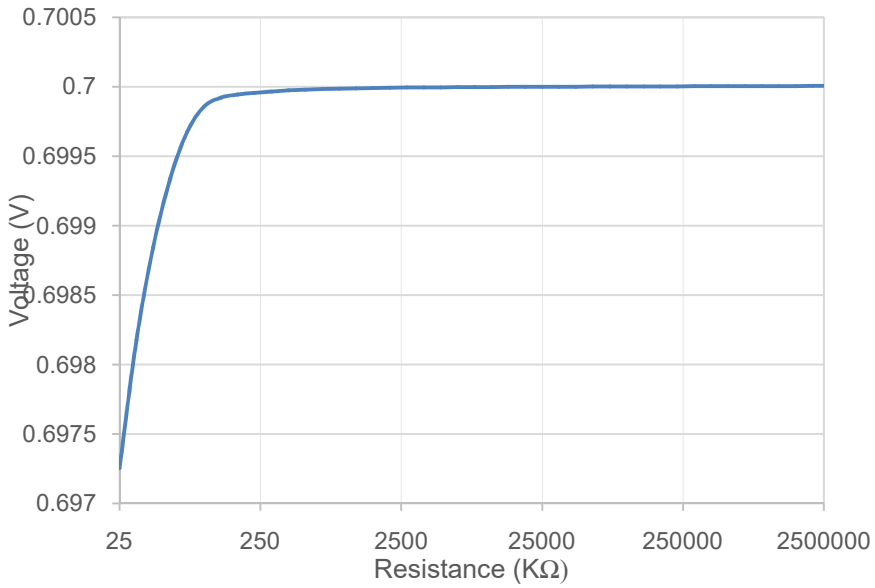


Figure 42: Difference between the voltages across WE and RE.

3.4.2 Feedback Stability

Stability analysis was performed for the potential control loop consisting of electrochemical equivalent circuit and transistor $M_a$in the opamp feedback using I_{probe} and by varying R_{WE} over a wide range from 25 kΩ to 25GΩthat results in varied current out of the electrochemical sensor equivalent circuit and the resultant simulation characteristics were noted. Figure 43 to 46 shows the Bode plot of the closed loop gain and phase for working electrode resistance of 1 GΩ, 25 MΩ, 100 kΩ and 20 kΩ respectively. Table 5 summarizes their simulation results including Gain, Crossover Frequency, Phase Margin and the resultant output current of the current mirror.

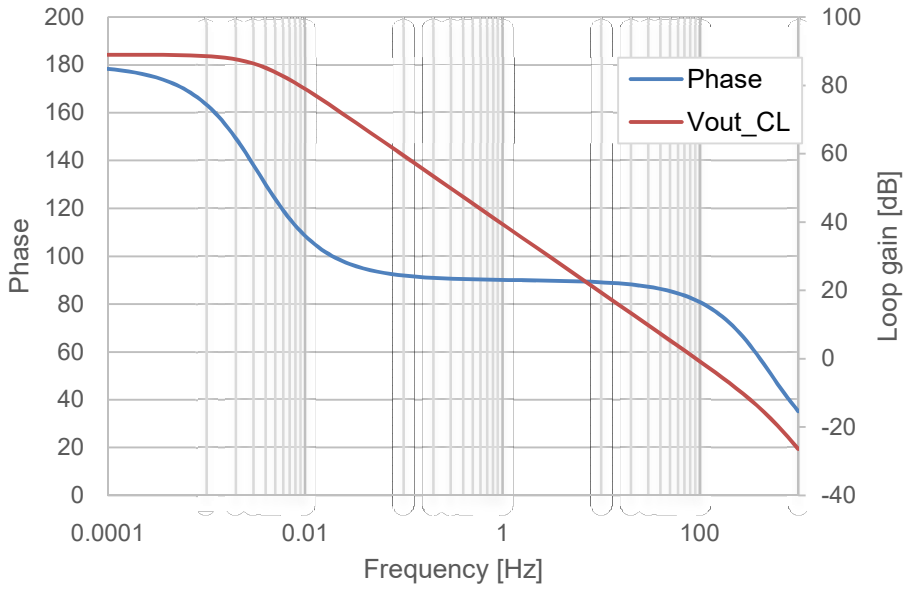


Figure 43: Control amplifier loop gain simulation with R_{WE}=1 GΩ.

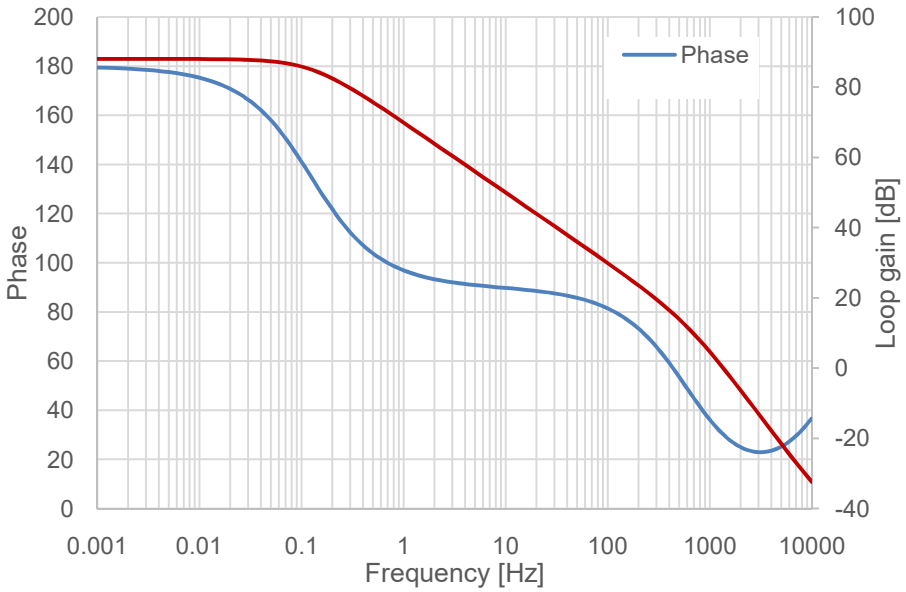


Figure 44: Control amplifier loop gain simulation with R_{WE}=25 MΩ.

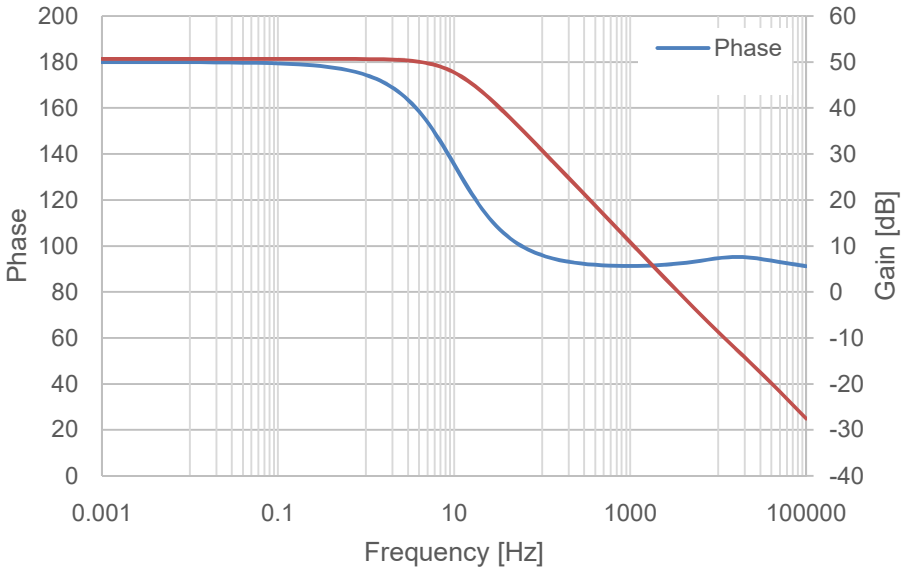


Figure 45: Control amplifier loop gain simulation with R_{WE}=100 kΩ.

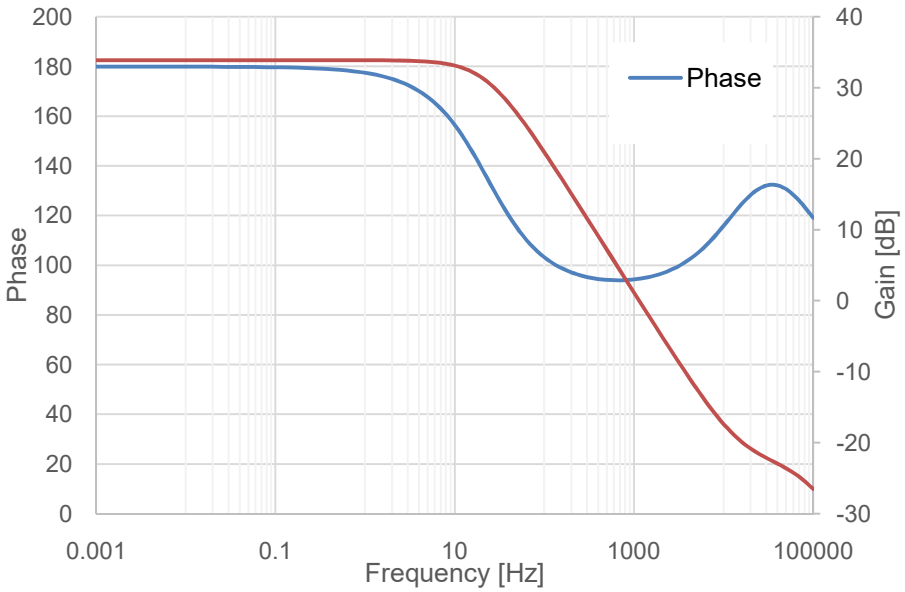


Figure 46: Control amplifier loop gain simulation with R_{WE}=20 kΩ.

Table 5: Stability Analysis Simulation Characteristics of the Potential Control Loop

	Gain [dB]	Crossover Frequency	Phase Margin	Output Current (A)
20 k	27.3	600 Hz	94.44˚	34.838 µ
25 k	33.9	1.14 kHz	94.56 ˚	27.910 µ
100 k	50.68	3.51 kHz	92.23˚	6.9999 µ
500 k	84.64	5.81 kHz	25.85˚	1.4001 µ
1 M	86	4.86 kHz	23.44˚	700.11 n
25 M	88.1	1.35 kHz	30.21˚	28.012 n
1 G	90	92 Hz	81.52˚	703.63 p
7G	89.20	13.73 Hz	88.05˚	104.27 p

3.4.3 Offset Simulation of the Potentiostat

In this section, the offset between the two input ports of the control amplifier in the potentiostat structure has been simulated using the Monte Carlo analysis and mismatch simulation. This offset represents the variation of the (V_{WE}-V_{RE}) by process and mismatch variation. The simulation result is shown in Figure 47 for R_{WE}=2 MΩ. The result predicts a maximum mismatch of 7.57 mV.

The offset value was also measured for varying values of R_{WE}. The offset is expected to decrease with decreasing sensor current, therefore it decreases with increase in R_{WE}. The offset is affected by varying loop gain due to varying working electrode resistance over a wide range in the feedback loop. Figure 48 shows the plot of offset results for varying R_{WE}. The maximum offset voltage variation is 2.045 mV.

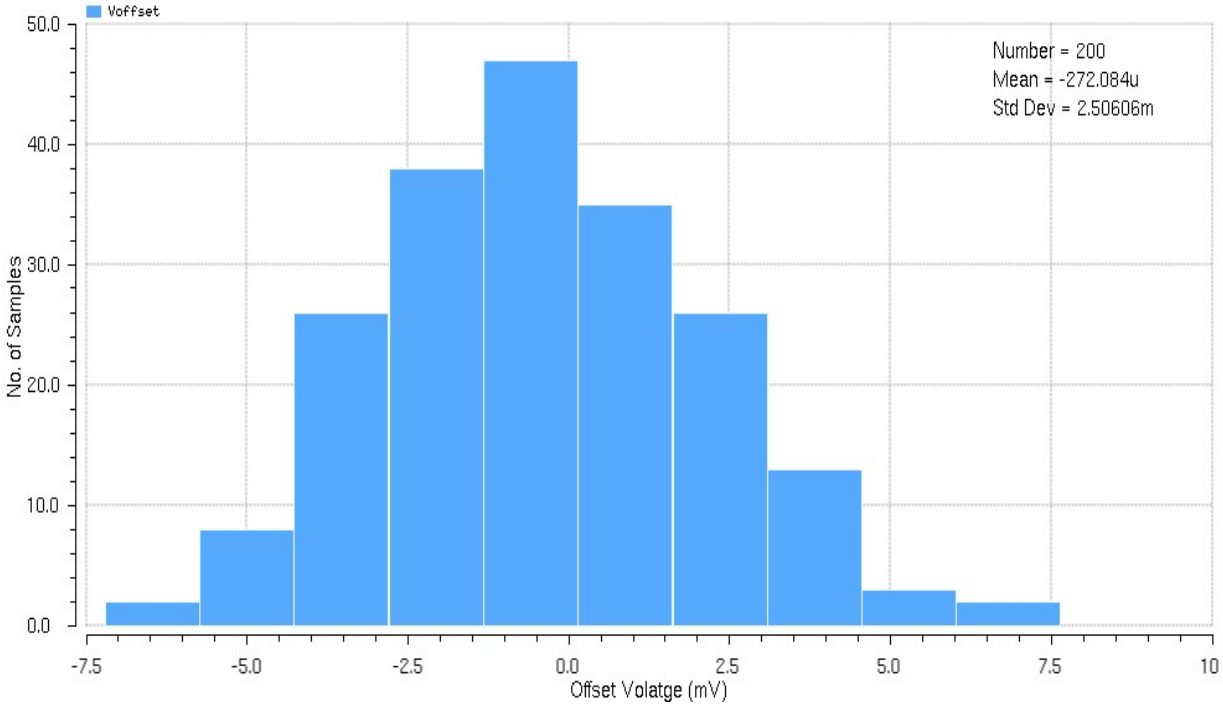


Figure 47: Offset between two inputs of the control amplifier in the potentiostat structure which also represents the variation of (V_{WE}-V_{RE}) by process and mismatch variation.

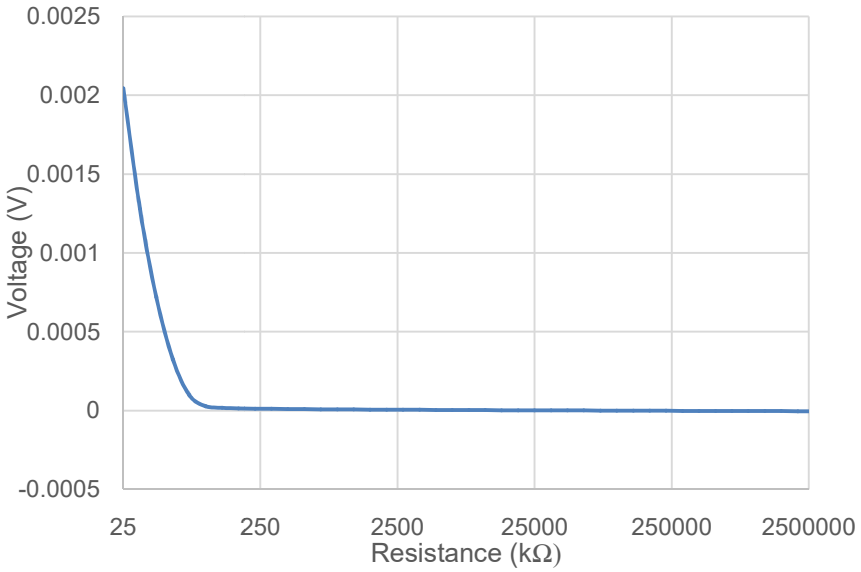


Figure 48: Offset measurement results for varying R_{WE}.

3.4.3 Output Voltage

The final output voltage from the transimpedance amplifier was plotted against varying working electrode resistance. The output is referenced to 900mV which was fed to the positive terminal of the TIA. For smaller currents, the change in output voltage was very small and hence three different feedback resistor values were used. The use of a transimpedance amplifier is optional. The sensor current can be measured from the current mirror directly. Table 6 shows the output voltage range for a different range of R_{WE}. Figures 49 and 50 show the plot of output voltage versus varying R_{WE}.

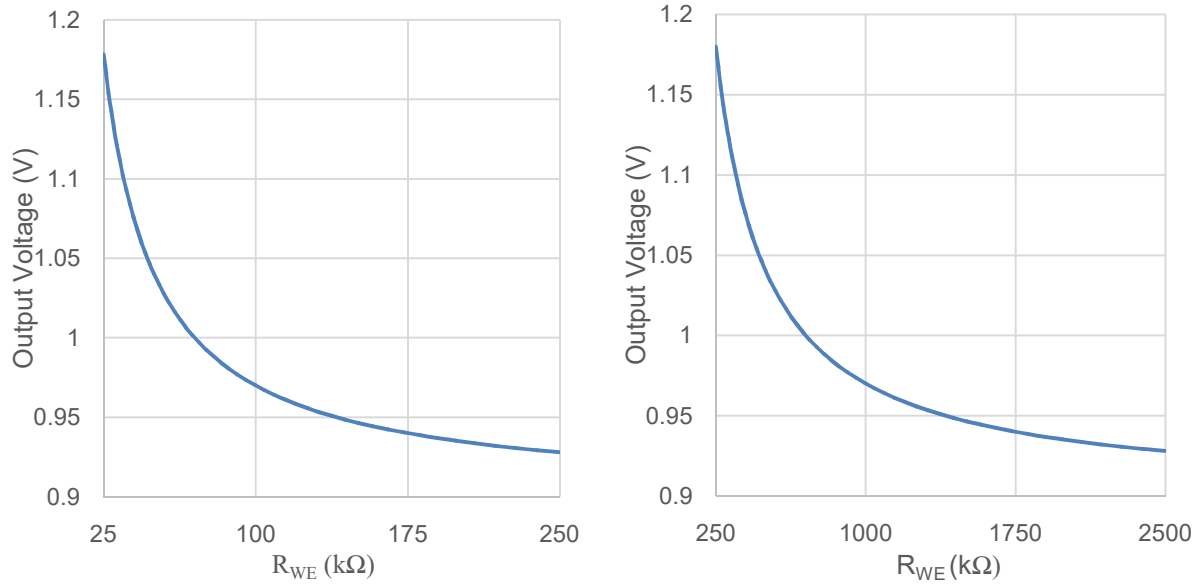


Figure 49: Plot of Output voltage versus varying R_{WE}

(a) For R_{WE}= 25 kΩ - 250 kΩ and R_F =10 kΩ b) For R_{WE}= 250 kΩ - 2.5 MΩ and R_F =100 kΩ.

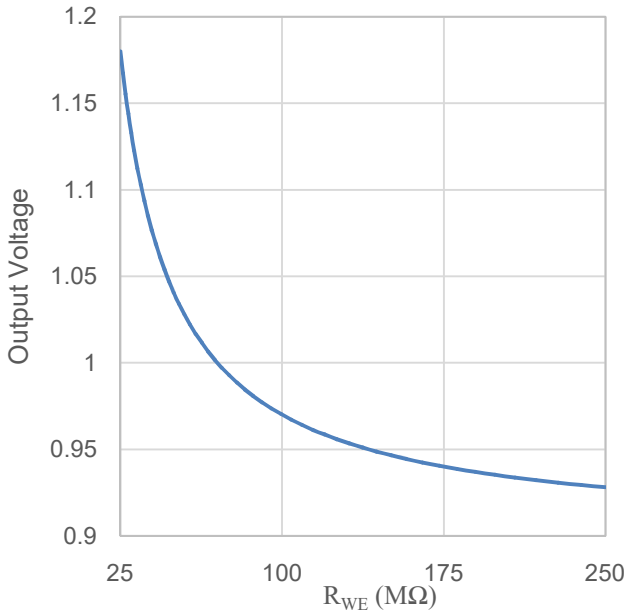


Figure 50: Plot of Output voltage versus R_{WE} for R_{WE}= 2.5 MΩ - 25 MΩ and R_F=1 MΩ.

Table 6: Output Voltage Simulation

R_{WE}(Ω)	R_F(Ω)	Output Voltage (V)
25 k – 250 k	10 k	1.1783 – 0.9279
250 k – 2.5 M	100k	1.1802 – 0.9283
2.5 M – 25 M	1M	1.1800 -0. 9280

3.4.5 Accuracy

The percentage error between the sensor current I_{sensor} and output of the current mirror I_{out} was calculated using equation 16 as shown below:

$$\text{Percentage Error} = \frac{\text{Isensor-Iout}}{\text{Isensor}} \times 100 \quad (16)$$

Figure 51 shows the percentage error when the sensor current (I_{sensor}) is varied from 100 pA to 10 µA. It has a worst case error of 0.37% in the range 1nA to 10µA and a worst case error of 4.27% for the range 100 pA to 10 µA.

3.4.4 Linearity of the sensor current

Figure 52 shows the simulated I_{sensor} and I_{out} that is input sensor current and output of the current mirror in the range of 100 pA to 1 µA. A linear regression line is used to fit the simulation results to evaluate the accuracy and linearity. The result shows that the circuit exhibits excellent linearity with R^2 =0.999999999961.

3.4.5 Power Consumption

Table 7 summarizes the power consumption of the potentiostat for varying R_{WE}, with and without TIA.

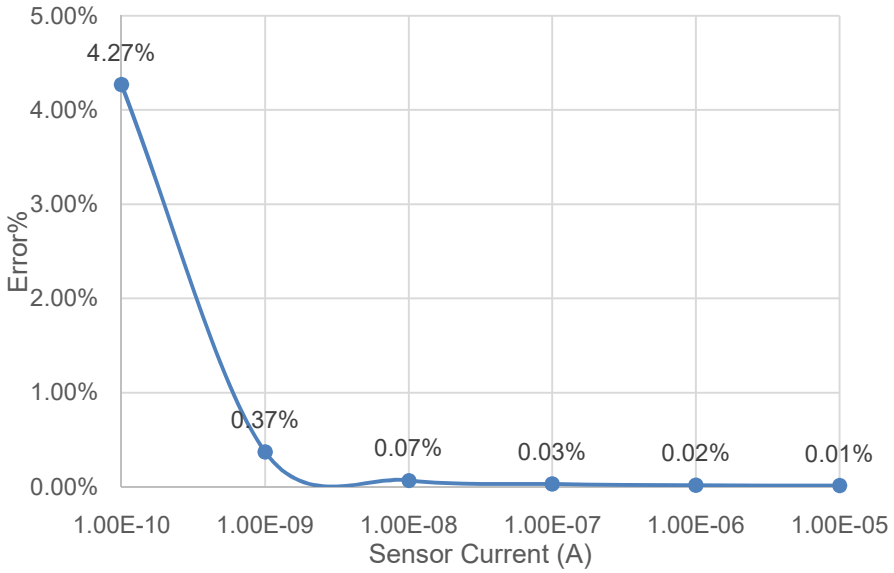


Figure 51: Simulated percentage current error.

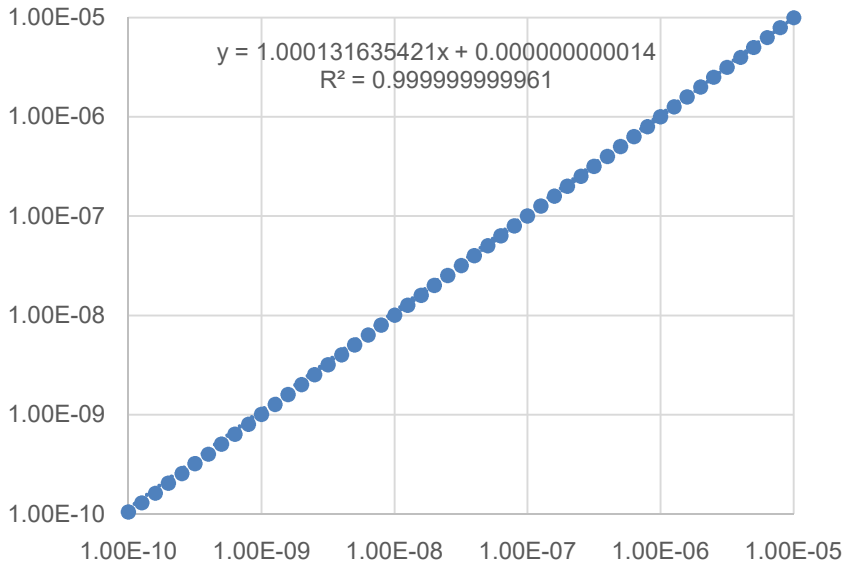


Figure 52: Linearity of the simulated sensor current.

Table 7: Power Consumption Summary

R_{WE} (Ω)	Power consumption without TIA (µW)	Power consumption with TIA (µW)
70 k	51.9	115
700 M	75.6	140.006
7 G	76.6	141.118

CHAPTER 4- PHYSICAL LAYOUT DESIGN AND POST LAYOUT SIMULATION

4.1 Physical Layout Design

All the circuits were verified using schematic level simulation and the layouts were designed in 0.18µm PDK using Cadence Virtuoso Layout Suite XL. Each layout cell was verified using Mentor Graphics Calibre software and the PDK provided rule decks: Design Rule Check (DRC) and Layout Versus Schematic (LVS). The figures below show the Cadence layouts of different blocks.

The Cadence layouts shown in Figures 53 to 57, consisting of:

- Figure 53 Layout of the control amplifier
- Figure 54 Layout of the V_{GS}-multiplier LVCCM
- Figure 55 Layout of the TIA
- Figure 56 Layout of the potentiostat
- Figure 57 Layout of the potentiostat with pads

The chip was shared with 3 other students. The total area consumption of the entire Potentiostat is 0.012 mm^2 without the TIA and 0.017 mm^2 with the TIA. Figure 57 shows the final potentiostat with the pads and also includes the layouts of the other students. Each hierarchy of design was placed and routed until the top level was completed, and then placed and routed into a pad frame with ESD protected pads. Fill materials were then added to the empty space and a seal ring was added to meet the fabrication foundry requirements. The completed chip layout was then submitted for fabrication.

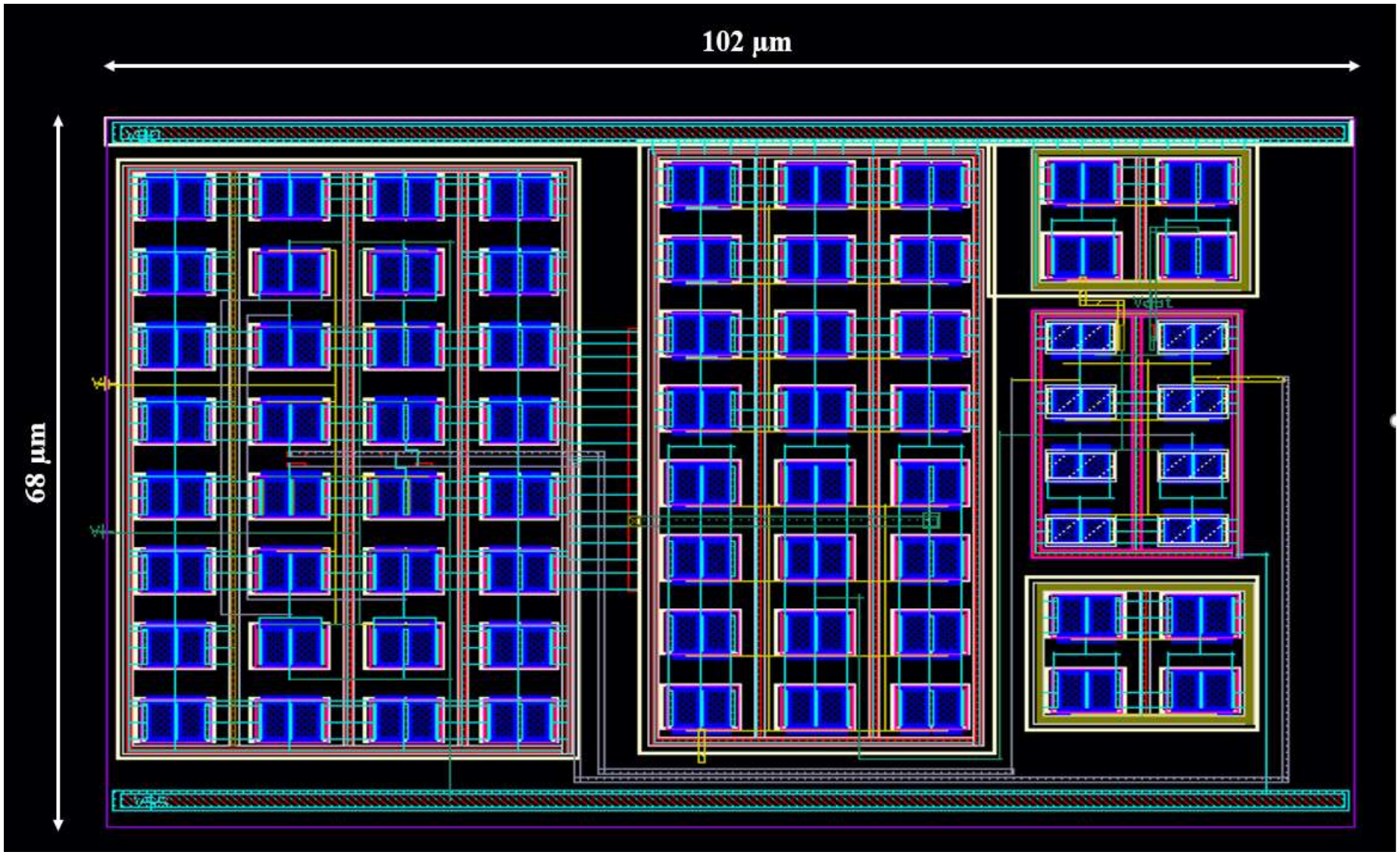


Figure 53: Layout of the control amplifier.

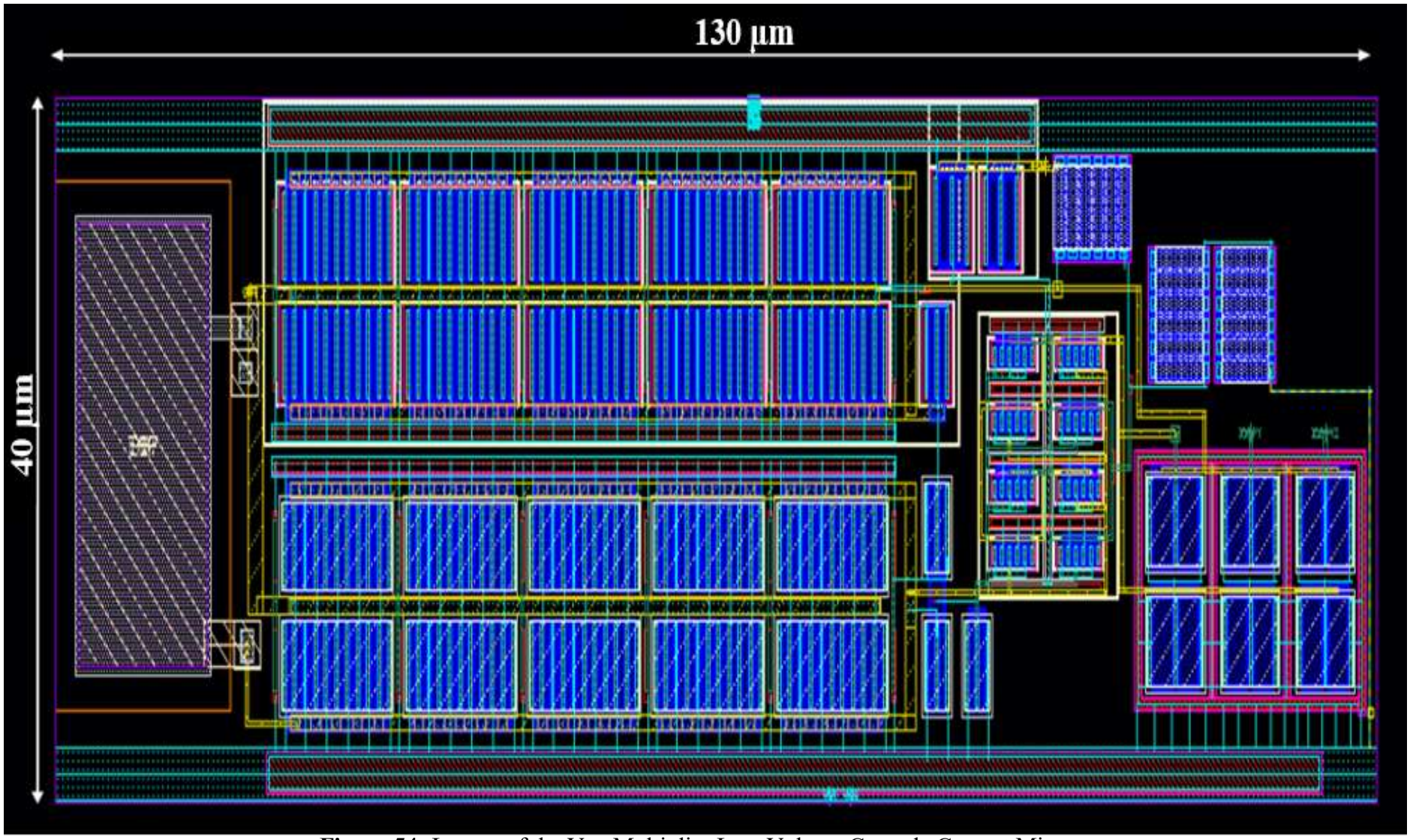


Figure 54: Layout of the V_{GS}-Multiplier Low Voltage Cascode Current Mirror**.**

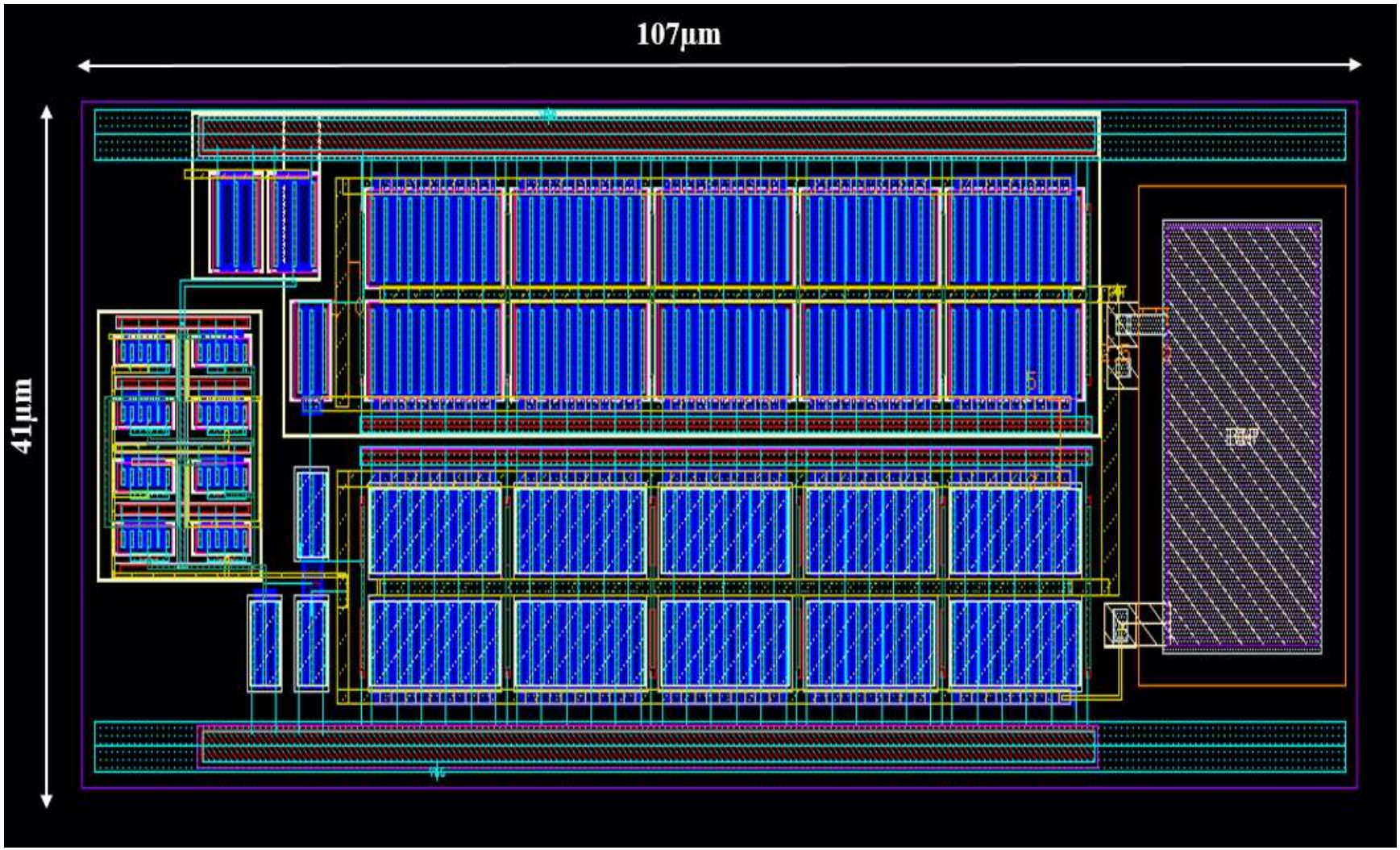


Figure 55: Layout of the Transimpedance Amplifier opamp.

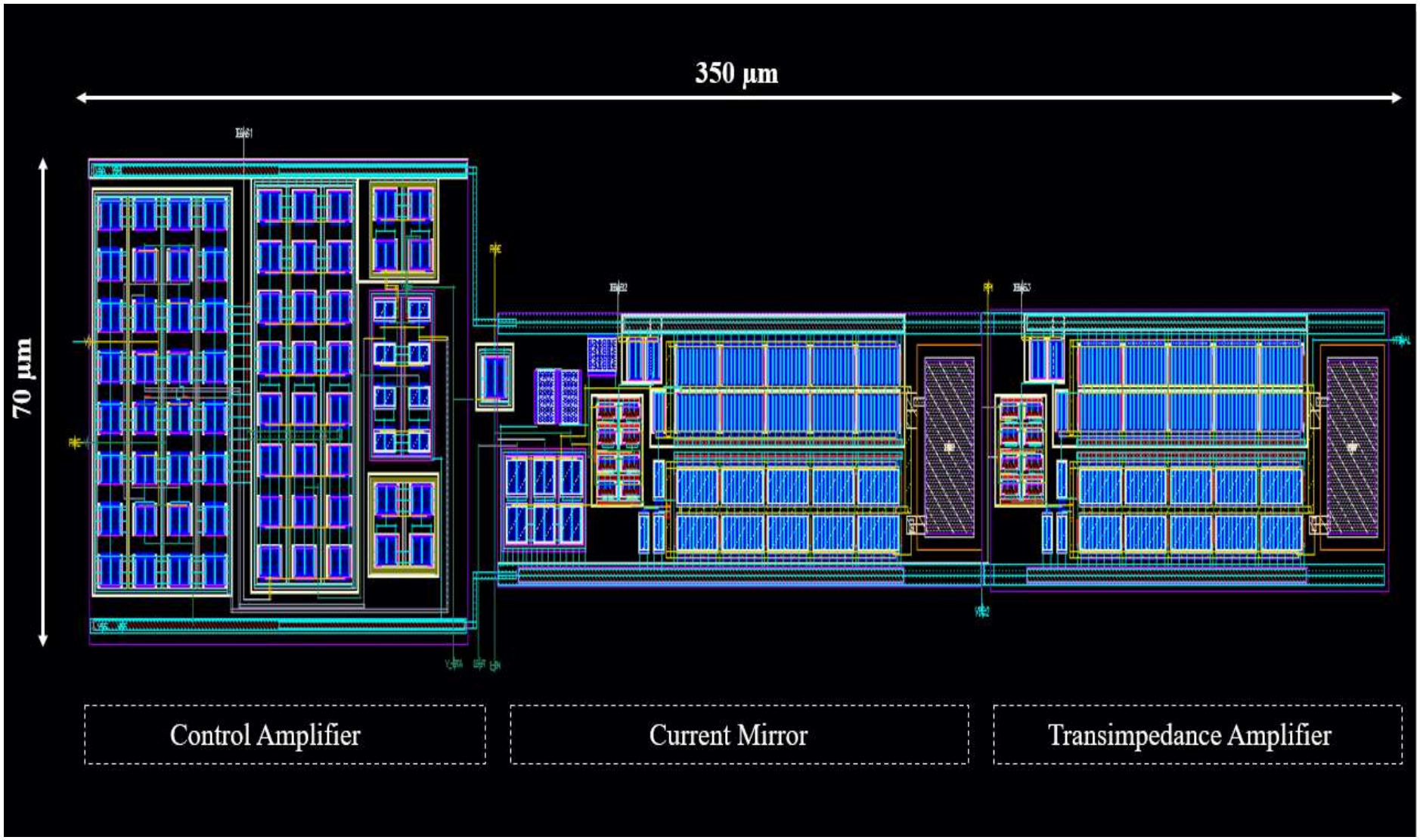


Figure 56: Layout of the potentiostat.

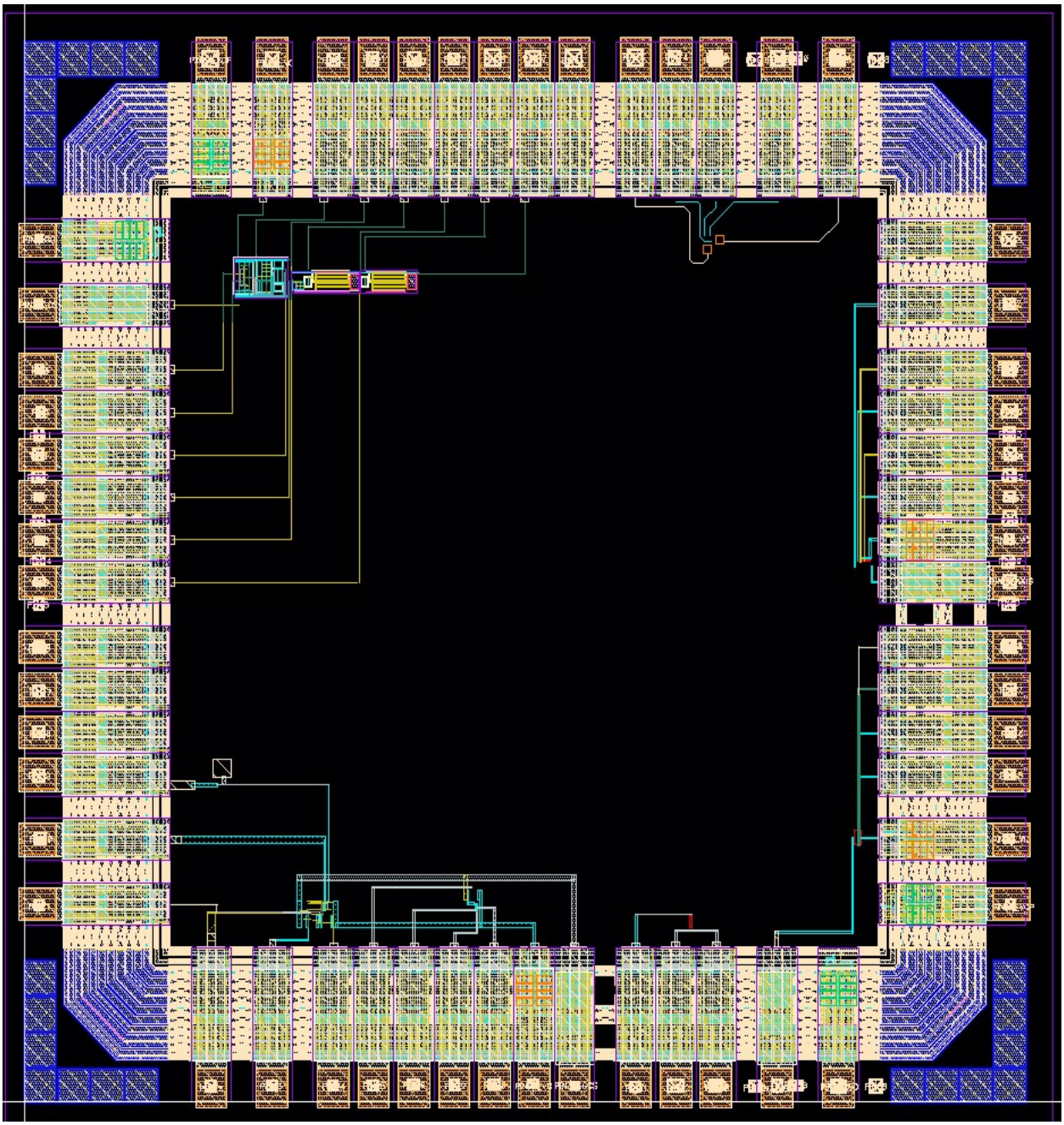


Figure 57: Layout of the potentiostat with pads – 2 mm × 2 mm.

4.2 Post Layout Simulations

4.2.1 Electrode Voltages

As mentioned in the performance summary of the Potentiostat section, the voltages across WE and RE must be constant and is verified by post layout simulations. Figure 58 shows the voltages across working and reference electrodes for varying resistance from 25 kΩ to 25GΩ.Figure 59 shows the difference in potentials across electrodes for varying resistance in the same range.

4.2.2 Feedback Stability

The potential control loop was simulated again post layout, varying R_{WE} over a wide range from 25 kΩ to 25 GΩ which resulted in varied current out of the electrochemical sensor equivalent circuit and the resultant simulation characteristics are as shown in Table 8. Figures 60 to 63 show the Bode plot of the closed loop gain and phase for working electrode resistance of 1 GΩ, 25 MΩ, 100 kΩ and 20 kΩ, respectively. It is evident from the result that post layout simulations agree with schematic simulation results.

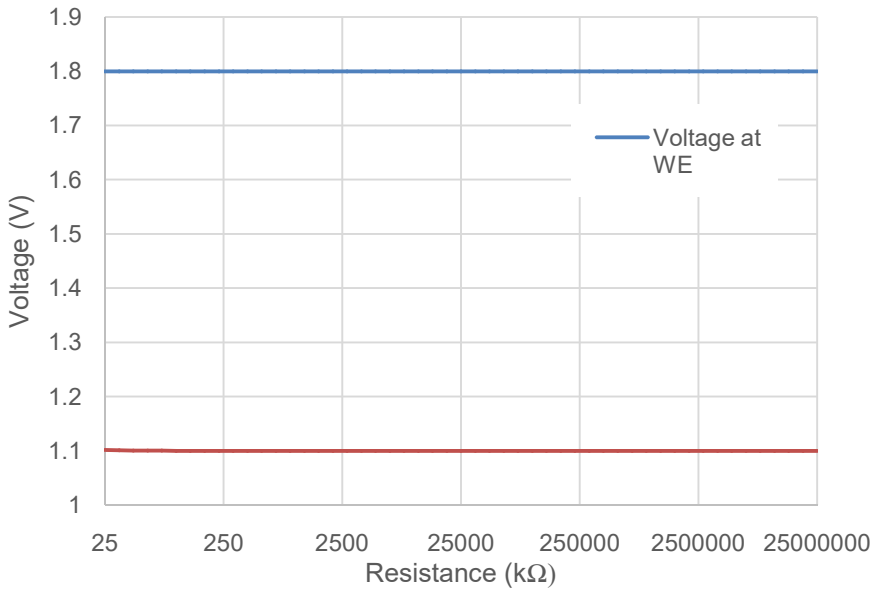


Figure 58: Voltages at the Working electrode and Reference electrode versus $R_{WE.}$

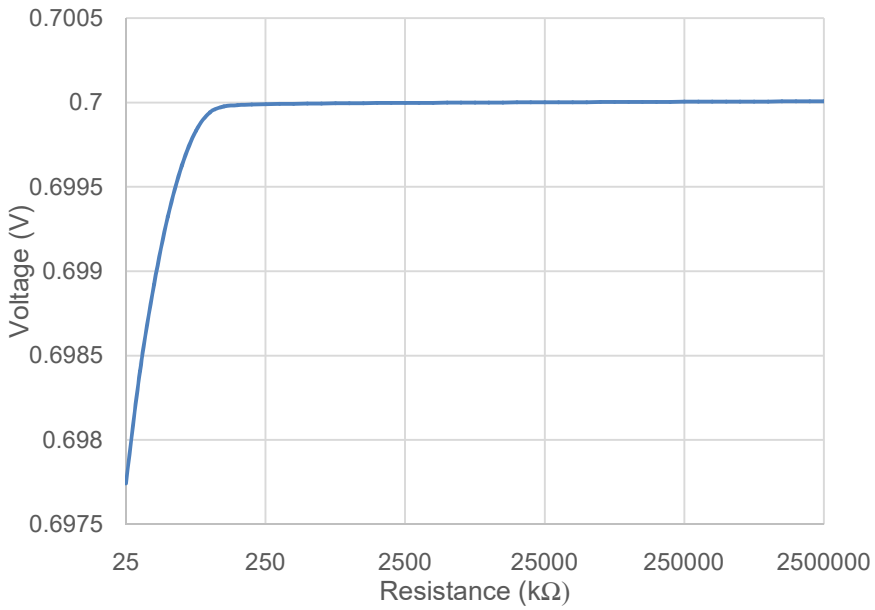


Figure 59: Difference between the voltages across WE and RE versus R_{WE} post layout.

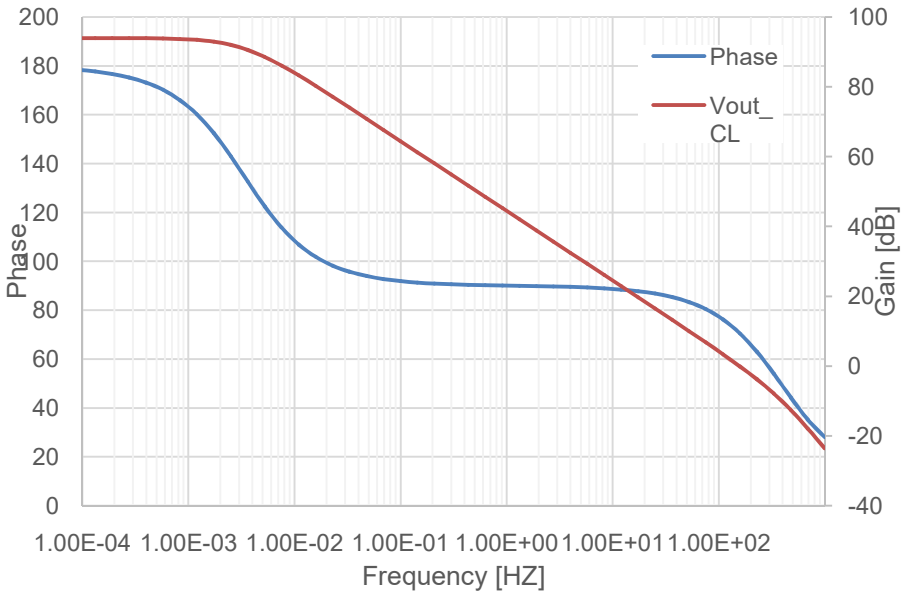


Figure 60: Control amplifier loop gain simulation with R_{WE}=1 GΩ.

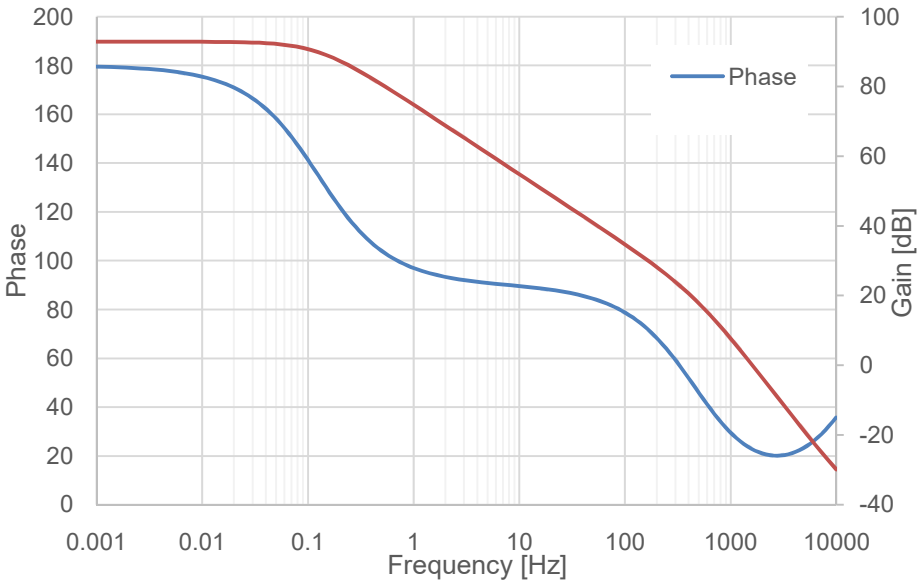


Figure 61: Control amplifier loop gain simulation with R_{WE}=25 MΩ.

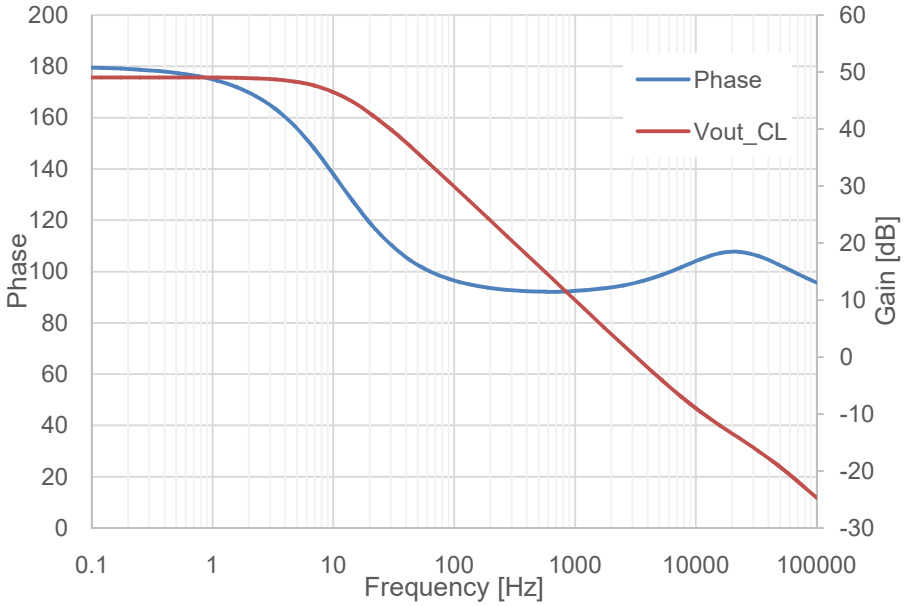


Figure 62: Control amplifier loop gain simulation with R_{WE}=100 kΩ.

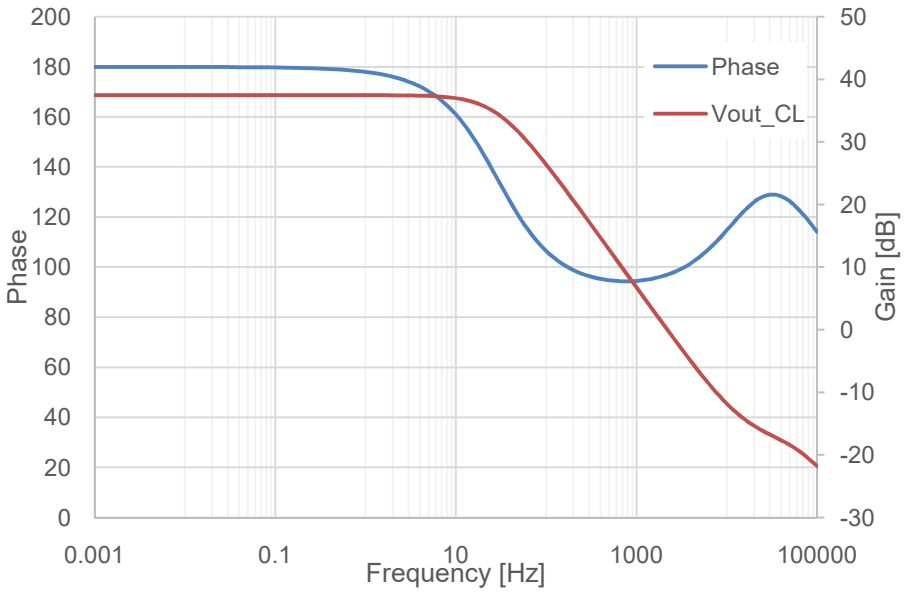


Figure 63: Control amplifier loop gain simulation with R_{WE}=20 kΩ.

Table 8: Stability Analysis Simulation Characteristics of Potential Control Loop Post Layout

Resistance (Ω)	Gain [dB]	Cut-Off Frequency	Phase Margin	Output Current (A)
20 k	37.49	2.209 kHz	97.01˚	34.942 µ
25 k	39.36	2.415 kHz	97.13 ˚	27.970 µ
100 k	49.06	3.192 kHz	95.61˚	7.0010 µ
500 k	88.11	7.310 kHz	29.05˚	1.4000 µ
1 M	90.16	5.960 kHz	25.26˚	700.21 n
25 M	92.88	1.600 kHz	22.71˚	28.016 n
1 G	93.99	157.1 Hz	70.66˚	705.04 p
7 G	94.45	24.56 Hz	85.12˚	105.97 p

4.2.3 Output Voltage

The final output voltage from the transimpedance amplifier was simulated post layout for varying R_{WE}. The output is referenced to 900mV that is fed to the positive terminal of the TIA. Similar to the schematic simulation, three different feedback resistor values were used for different range of sensor currents. Table 9 summarizes the output voltage range for varying R_F range. Figure 64 and 65 show the output voltage for varying R_{WE}.

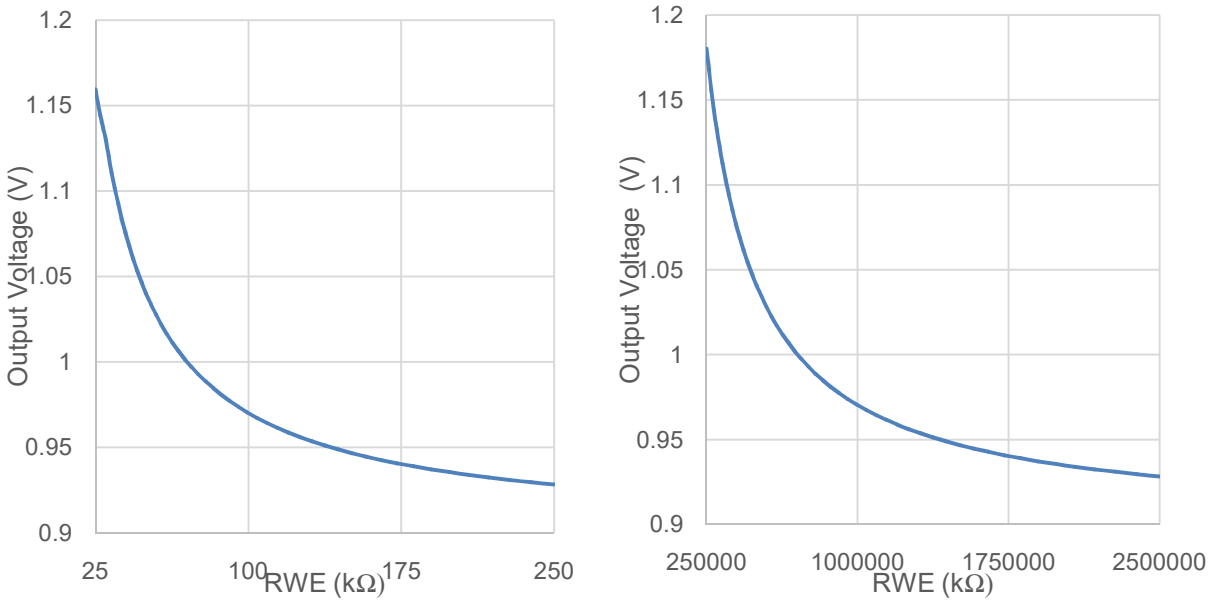


Figure 64: Plot of Output voltage versus R_{WE}

a) For R_{WE}= 25 kΩ - 250 kΩ and R_F=10 kΩ b) For R_{WE}= 250 kΩ - 2.5 MΩ and R_F=100 kΩ

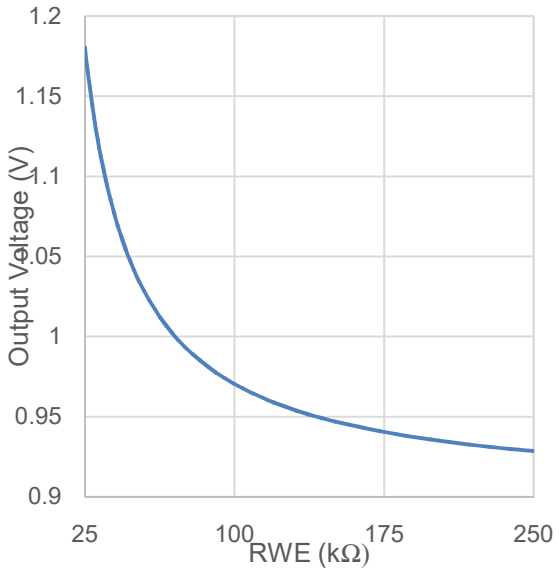


Figure 65: Plot of output voltage versus R_{WE} for R_{WE}= 2.5 MΩ - 25 MΩ and R_F=1 MΩ.

Table 9: Output voltage post layout simulation

R_{WE}(Ω)	R_F (Ω)	Output Voltage (V)
25 k – 250 k	10 k	1.1594 – 0.9282
250 k – 2.5 M	100k	1.1799 – 0.9280
2.5 M – 25 M	1M	1.1804–0.9283

4.2.4 Offset

The offset value was measured post layout for different values of R_{WE} which results in different values of sensor current. The worst case offset voltage is 1.301mV at 25 kΩ. Figure 66 shows the plot of offset voltage versus R_{WE}.

4.2.5 Accuracy

The percentage error between sensor current and output of the current mirror (I_{out}) was calculated again post layout using the equation as in schematic simulation. Figure 67 shows the percentage error when the sensor current (I_{sensor}) is varied from 100 pA to 10 µA. It has a worst case error of 0.51% for the range 1 nA to 10 µA at 1 nA and a worst case error of 5.97% for the range 100 pA to 10 µA at 100 pA.

4.2.6 Linearity

Figure 68 shows the post layout simulated I_{sensor} and I_{out} that is input sensor current and output of the current mirror in the range of 100pA to 1 µA. The result shows that the circuit exhibits excellent linearity with R^2 =0.9999999981.Figure 69 shows the Monte Carlo Analysis with 3σ Mismatch

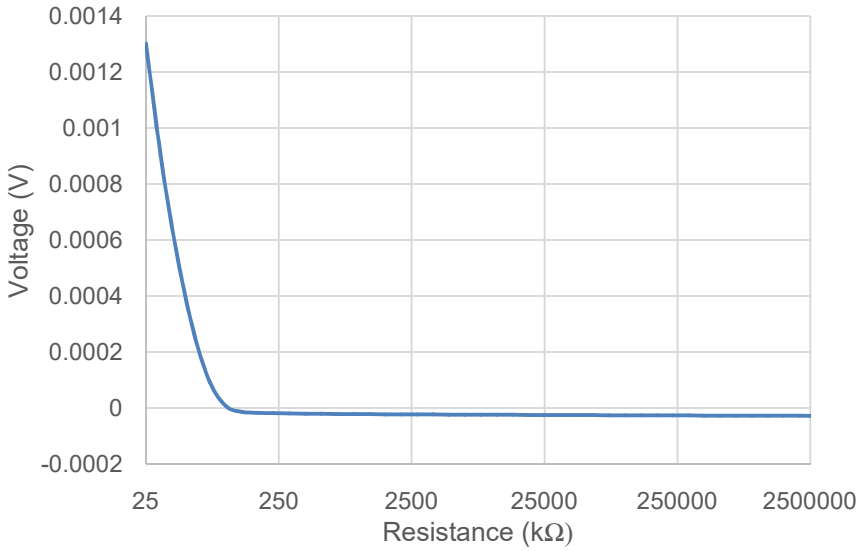


Figure 66: Plot of offset voltage versus working electrode resistance.

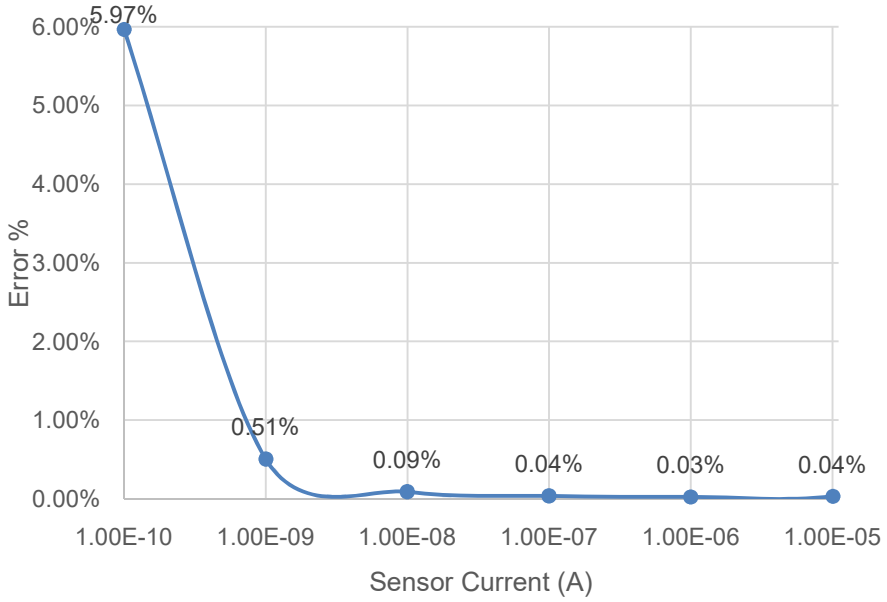


Figure 67: Post layout simulated percentage current error.

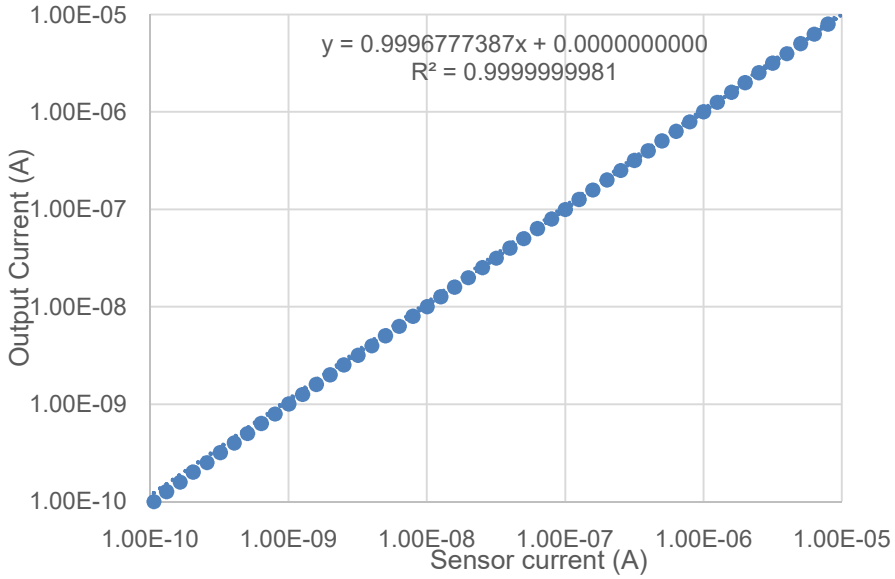


Figure 68: Linearity of the post layout simulated sensor current.

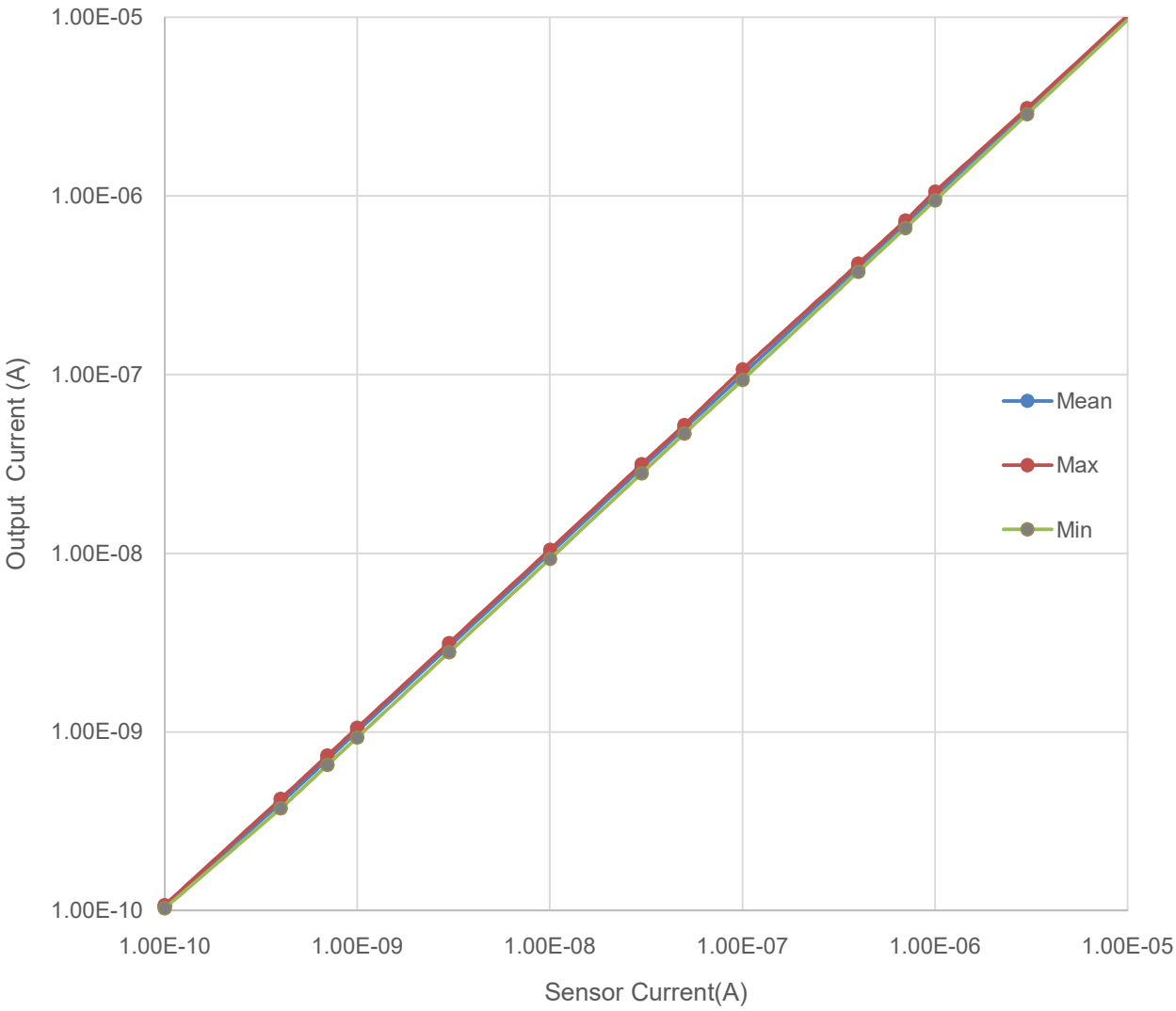


Figure 69: Monte Carlo analysis of the linearity with 3σ Mismatch.

CHAPTER 5- ATTEMPT OFEXPERIMENTAL VERIFICATION

5.1 Potentiostat Evaluation Board

In this chapter, the hardware and software test equipment's are explained in detail. The Potentiostat was fabricated in 0.18 μm, 1.8V CMOS process. The chip was hosted on an evaluation printed circuit board (PCB) via an open top socket. A pie filter was soldered next to the power supply pins to filter out AC ripples and the power supply noise. Specifically, ceramic capacitors of 0.1 μF and 100 μF were utilized to cover different bandwidth of the power supply noise. Another pair of pie filters was used for voltage source V_1 and V_2 to filter out the supply noise. The PCB test circuit was designed in Altium.

The Altium® schematics are shown in Figures 70 to 72, consisting of:

- Figure 70 PCB schematic of the proposed potentiostat Circuit
- Figure 71 3-D rendering of the Altium Design
- Figure 72 Potentiostat Evaluation board

Resistors were used to bias the different blocks of the potentiostats to set current biases. This resulted in increased range of sensor current that could be detected. So the new current range of potentiostat is 50 μA to 100 pA with a sensitivity of 14 pA. Additionally, from the definition of dynamic range D.R. = $20\log(I_{max}/I_{min})$, the proposed potentiostat circuit achieves a wider dynamic range of 113.97 dB.

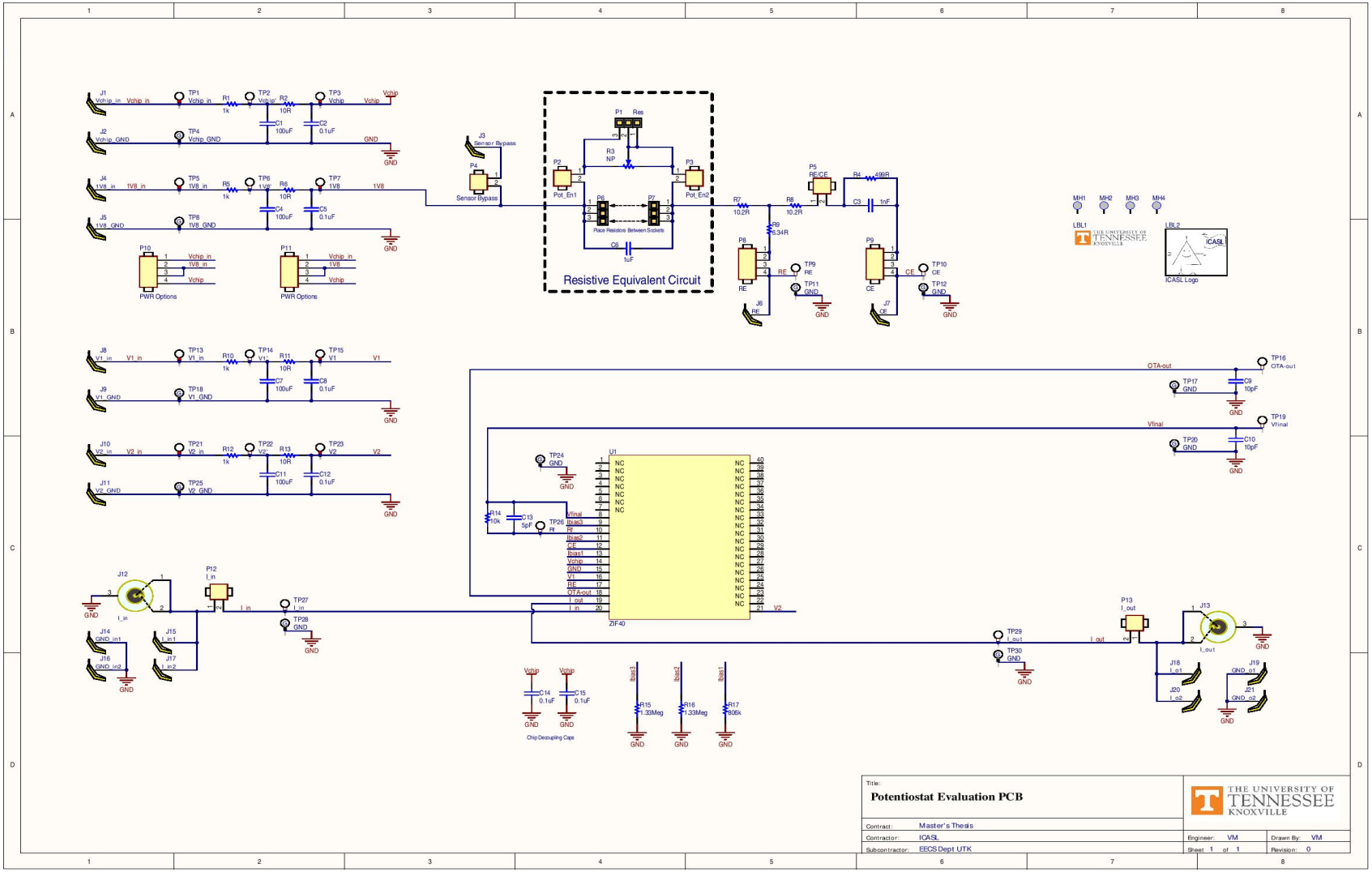


Figure 70: PCB schematic of the proposed potentiostat test circuit.

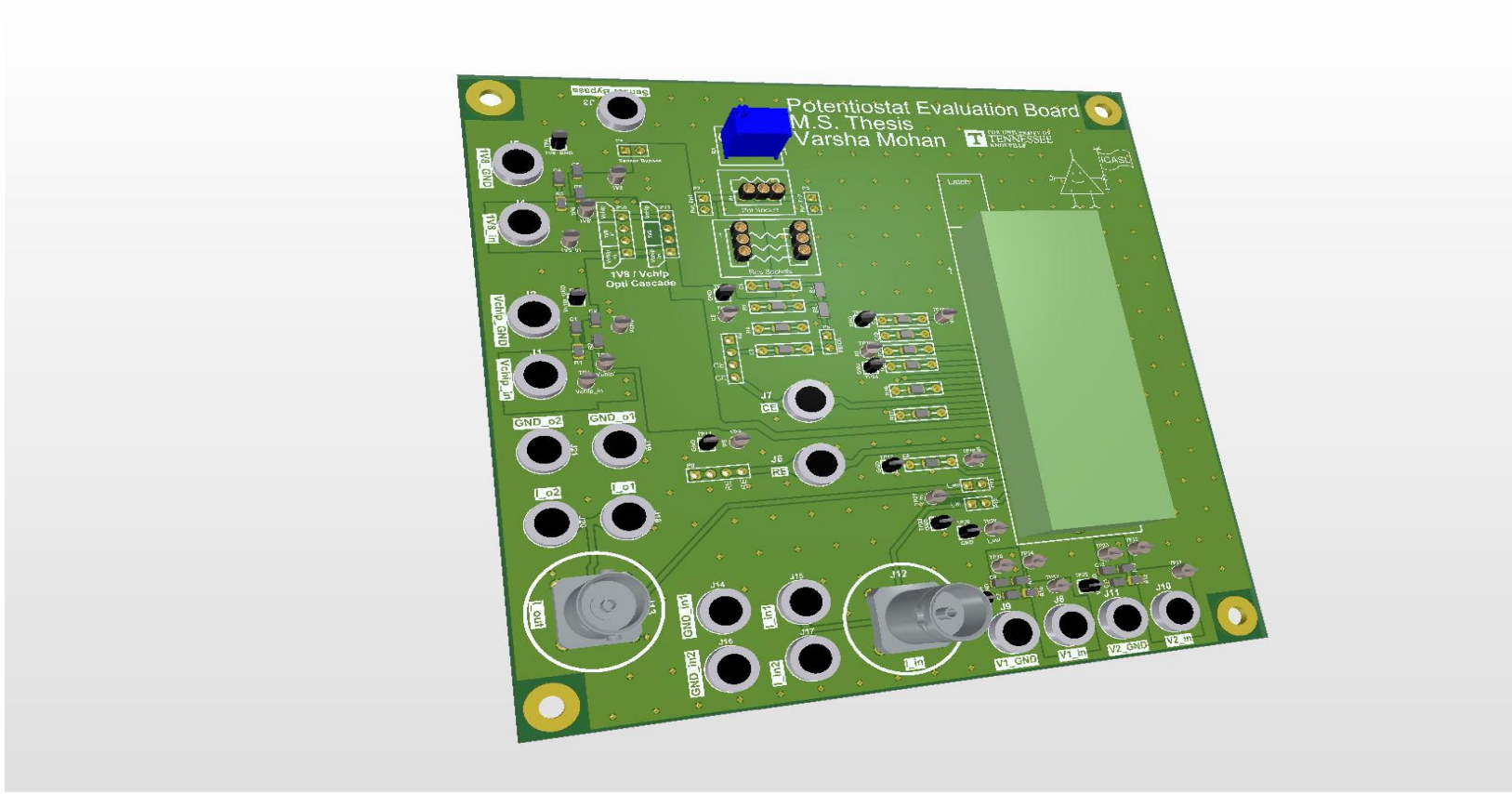


Figure 71:3-D rendering of the Altium Design.

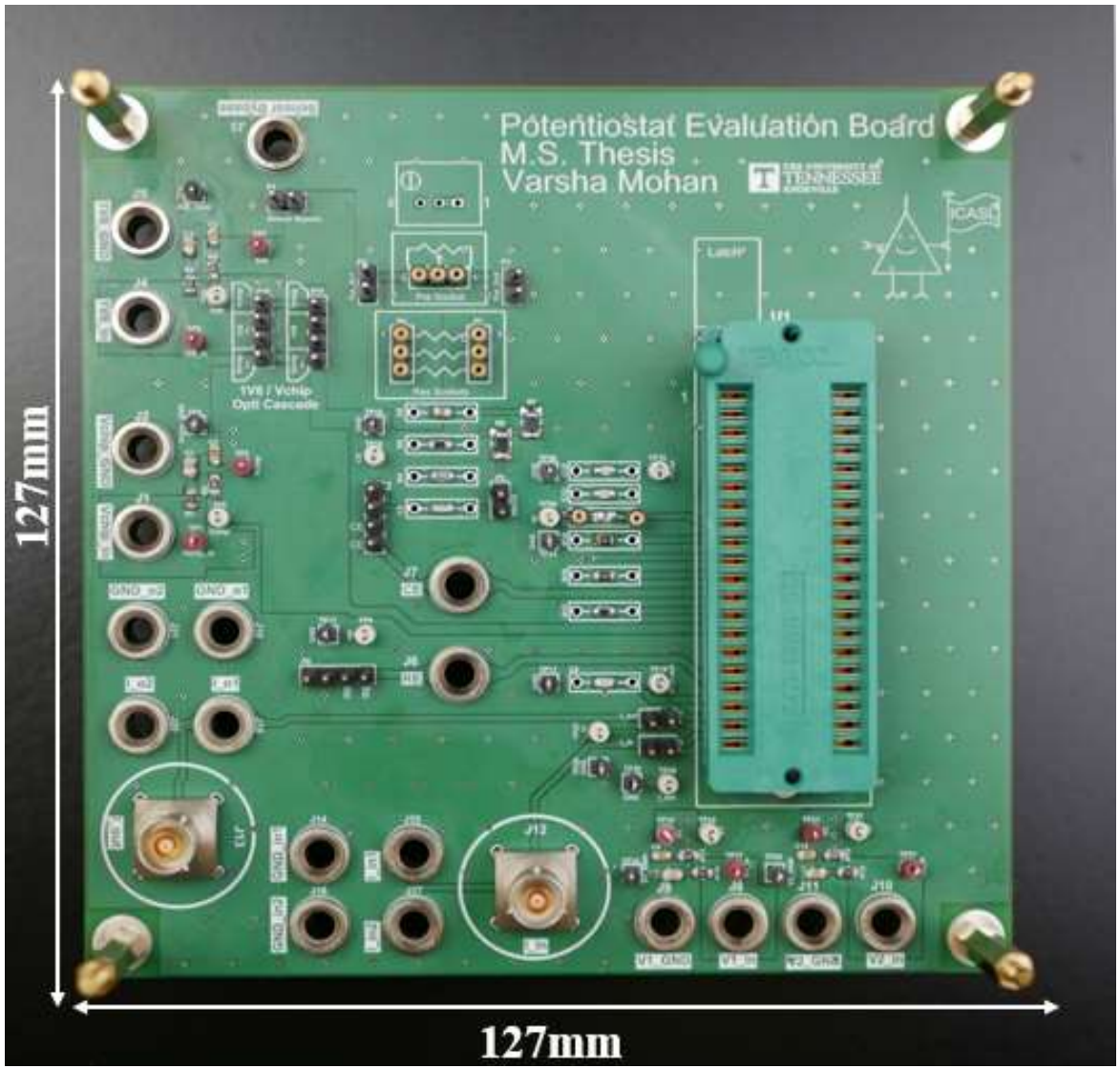


Figure 72: Image of the Potentiostat Evaluation Board.

5.2 Proposed Potentiostat Test Setup and Results

Figure 73 shows different testing blocks of the potentiostat evaluation board and Figure 74 shows the test setup. A triple power supply was used to provide supply voltage to the chip, bias voltage to the control amplifier and reference voltage to the TIA. A source meter with high resolution of Femto Amperes range was setup to measure the output current of the current mirror. Digital multimeters were used to measure the output voltage of the control amplifier, voltage at RE and final output voltage potentiostat/output of the TIA. The potentiostat Evaluation Board was designed to support the test with equivalent electrochemical circuit by placing sockets to switch the resistors as well to support standard electrochemical cell test by providing a bypass from the electrochemical equivalent circuit.

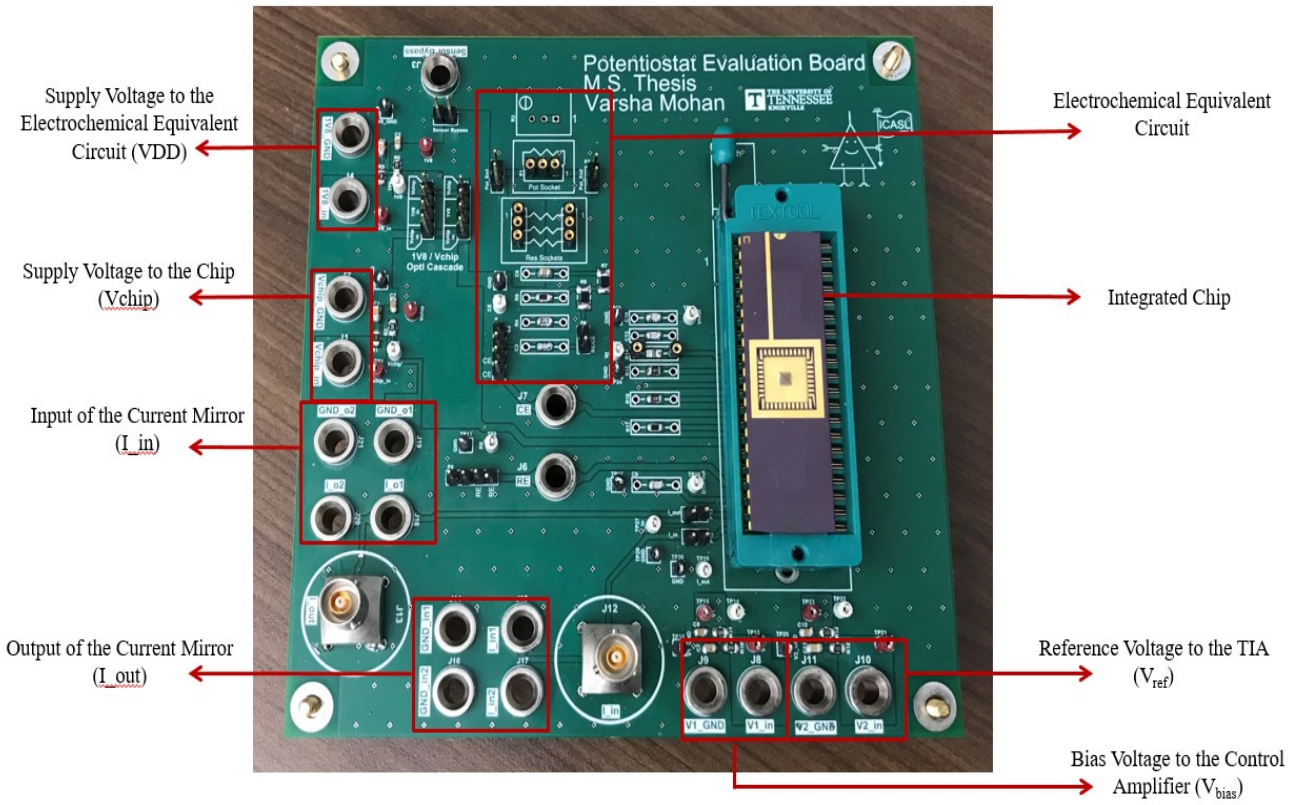


Figure 73: Potentiostat Evaluation board with different testing blocks.

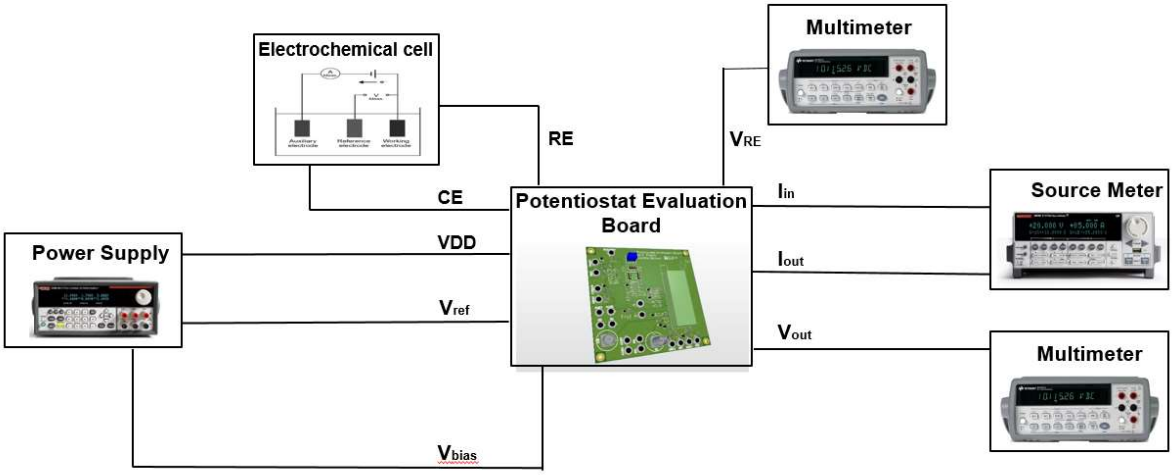


Figure 74: Potentiostat Evaluation board test setup.

The experiment was conducted with equivalent electrochemical circuit. The chip suffered ESD damage which resulted in current mirror and the TIA being completely off. Though ESD protection circuits were incorporated in the pad frame, the designs were connected to PADX which completely bypassed the ESD protection diodes. Hence the design was incapable of handling any ESD event.

Figure 75 shows the schematic of the ESD Circuit. The drains of ESD diode-connected MOSFETs are not directly connected to the core of the pad frame, they are connected to PADX and PAD by a current-limiting resistor. The ESD protection only works well when the design is connected directly to RIN (drains of ESD diode-connected MOSFETs). R1 and R2 are current limiting resistors. There is some very small parasitic resistance between PAD and PADX (33 μΩ).If the design is connected to PADX and RIN is floating, then an ESD event will discharge through the smallest resistance path to ground, which will be small resistance through PADX and the core design circuits. However, if PADX is left floating while the core design is connected to RIN, then an ESD event will have to discharge through the current limiting resistor and diode-connected MOSFETs before it can reach the core design circuits. Using PADX sacrificed the ESD protection and exposed design circuits to a human body discharge.

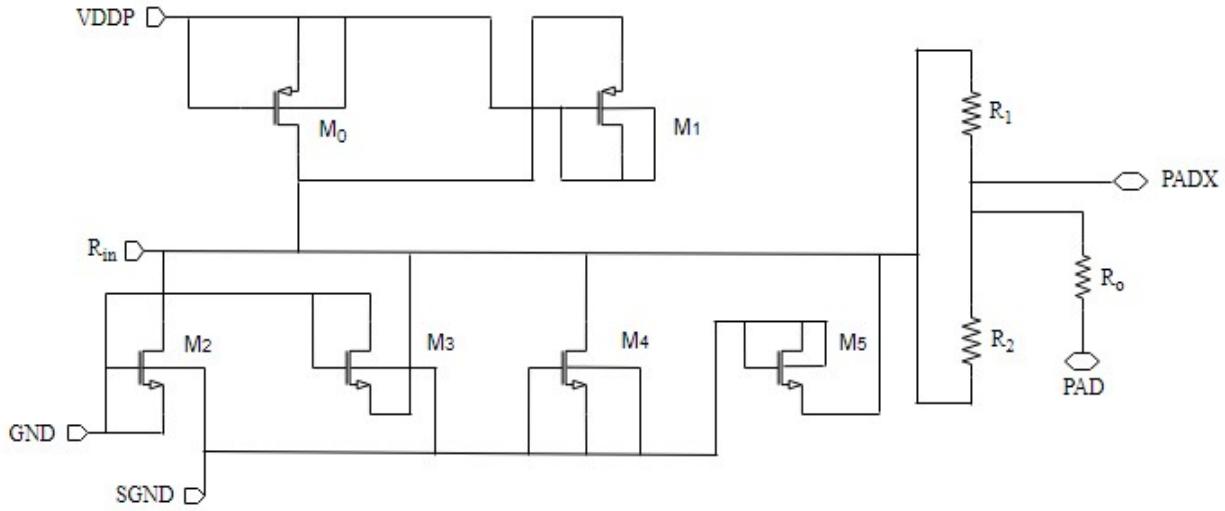


Figure 75: Schematic of the ESD Circuit.

One of the main functions of the potentiostat is to maintain constant potential between WE and RE. The potential control loop was activated by connecting I_{in} to the ground and the voltage at RE was measured for varying $R_{WE.}$ Figure 76 shows the voltage across working and reference electrodes for varying resistance from 12 kΩ to 12 GΩ. Figure 77 shows the difference in potentials across electrodes for varying resistance. The X-axis represents varying working electrode resistance. Y-axis represents the difference in voltage across WE and RE which starts with 0.698V for 12 kΩ and eventually settles to 0.7 V as the resistance increases. The measured results agree with the simulation results which prove that the implemented control amplifier with the potential control loop is stable. Table 10 summarizes the comparison of post layout simulation results with the previous work.

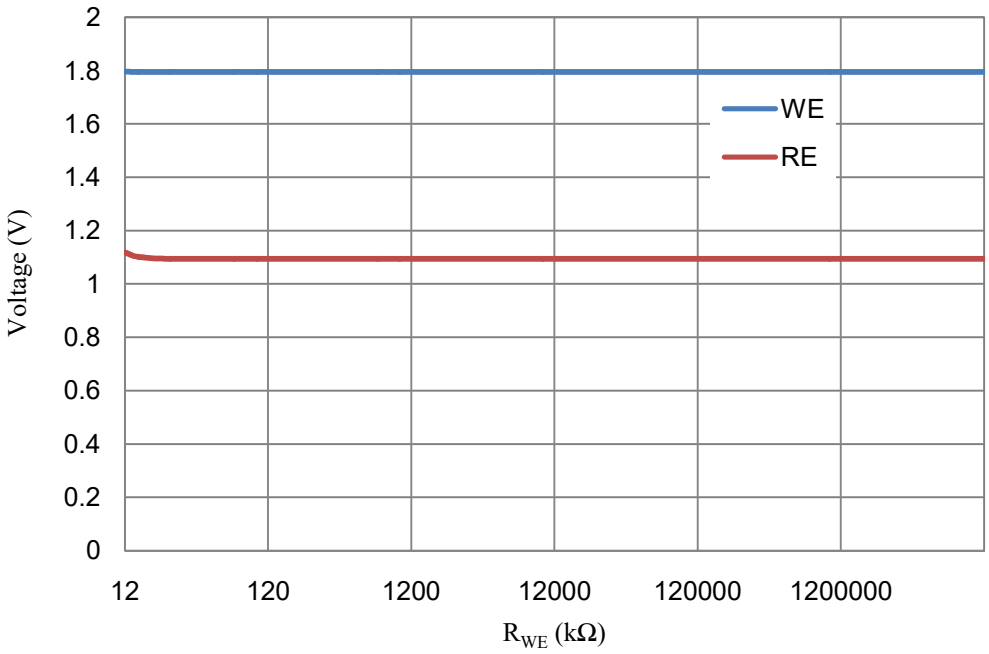


Figure 76: Measured voltage WE and RE for varying $R_{WE.}$

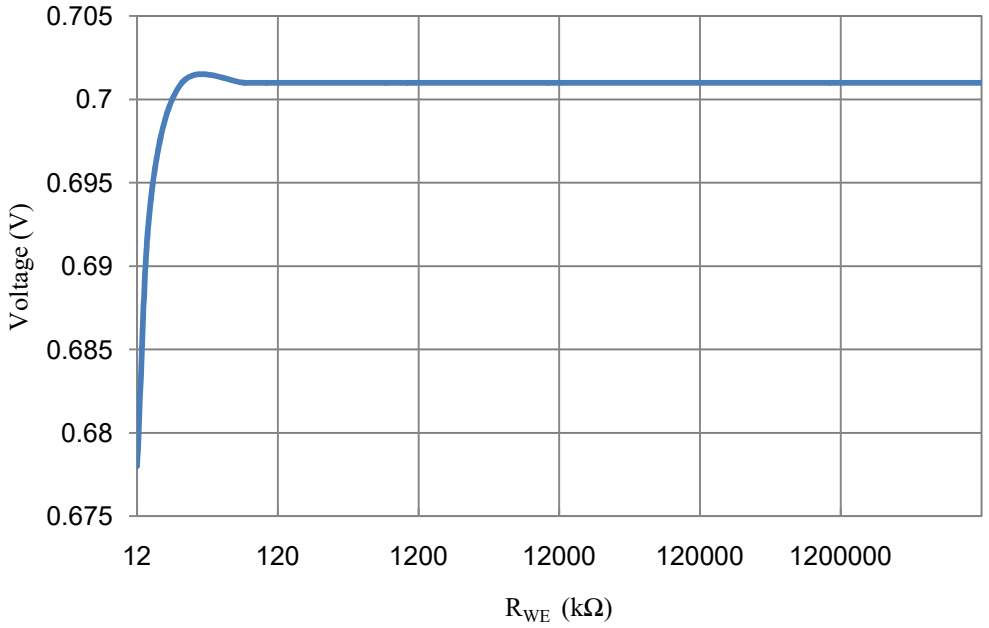


Figure 77: Measured voltage difference between the voltage at WE and RE.

Table 10: Comparison of post layout simulation results with previous work

	Supply Voltage (V)	Process	Sensor Current	Power Consumption	Linearity	Resolution	Area
This Work	**1.8**	**0.18 µm**	**50 µ - 100 pA**	**51 µW**	**0.9999999981**	**14 pA**	**0.012 mm^2 (w/o TIA)** **0.024 mm^2 (w/ TIA)**
[15]	1.8	0.18 µm	10 µA - 500 pA	1.24 mW	N/A	500 pA	0.066 mm^2
[17]	1.8	0.15 µm	1 µA - 10 nA	32 µW	0.99993	10 nA	Not Fabricated
[18]	1.8	0.35 µm	3 µA - 5 nA	10.2 µW	0.9908	N/A	0.013 mm^2
[19]	1	0.35 µm	2.6 µA -70 nA	22 µW	0.9941	70 nA	0.13 mm^2
[21]	1	0.18 µm	10 µA -1 nA	12.3 µW	0.99996	1 nA	Not Fabricated
[22]	3.3	0.35 µm	200 pA	398 µW	N/A	200 pA	N/A
[23]	5/1.8	0.18 µm	1 nA – 4 µA	27.5 µW	N/A	900 pA	0.36 mm^2
[24]	1.8	0.18 µm	500 nA – 7 µA	53µW	N/A	500 nA	0.017 mm^2
[25]	1.5	0.35 µm	2.8 µA	16.8 µW	N/A	100 pA	0.5 mm^2
[26]	5	0.5 µm	1.5 nA – 10 pA	4.85 mW	N/A	10 pA	0.306 mm^2

CHAPTER 6 - CONCLUSION AND FUTURE WORK

6.1 Conclusion

A potentiostat is an integral part of an electrochemical sensor. This work discusses the various potentiostat configurations and presents a highly accurate, low power CMOS potentiostat with wide dynamic range, reduced mismatch and improved measurement sensitivity in the measurement. The proposed system incorporates a folded cascade OTA with bump degeneration for control amplifier, V_{GS}-multiplier biasing technique for the low voltage cascode current mirror and two stage cascade opamp for TIA. The proposed potentiostat can not only be used in glucose sensor but also for other electrochemical sensing applications depending on the required input common mode range. The potentiostat has been implemented using a 0.18 μm standard CMOS process with total chip area of 0.017mm^2 including TIA and has a wide dynamic range of 114 dB with very high accuracy of 0.03% to 5.97% for the lowest current. The results show an output linear regression of R^2=0.9999999981 over the sensor current range from 100 pA to 50 μA. The proposed potentiostat has a high resolution of 14 pA and it is capable of handling temperature variations which makes it highly suitable for implantable sensors. Due to the errors in ESD – pad frame connections, the design could not be completely verified experimentally. The measured electrode voltages verified that the potential control loop was stable over the desired sensor current range.

6.2 Future Work

The design could be refabricated with proper ESD protection and the results could be verified experimentally by testing with the electrochemical cell. Also, the power consumption of the control amplifier, opamp within the current mirror and the TIA could be reduced further with suitable design modifications. The design could be tested with different sensors with different V_{cell} voltages ranging from 0.3 V to 1.3 V to validate the functionality in different electrochemical sensing systems.

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VITA

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